NAWCWPNS TP 8242

19th Annual Electronics Manufacturing Seminar Proceedings

Sponsored by
Manufacturing Engineering Division
Systems Engineering Department
and
Manufacturing Technology Training Center
Comarco, Inc.

FEBRUARY 1995

NAVAL AIR WARFARE CENTER WEAPONS DIVISION
CHINA LAKE, CA 93555-6001

Naval Air Warfare Center Weapons Division

FOREWORD (U)

The proceedings contained herein are compiled and published by the Naval Air Warfare Center Weapons Division (NAWCWPNS) as supporting documentation for the 19th Annual Electronics Manufacturing Seminar to be held 22–24 February 1995 and sponsored by NAWCWPNS, China Lake, Calif. This document is a compilation of information that was provided by both nongovernment and government sources.

This document, which was prepared for timely presentation, contains information developed primarily by sources outside NAWCWPNS. NAWCWPNS assumes no responsibility for technical or editorial accuracy.

Approved by
Dr. R. E. SMILEY, *Head*
Systems Engineering Department

Under authority of
D. B. McKINNEY
RAdm., U.S. Navy
Commander

Released for publication by
S. HAALAND, Head
NAWCWPNS Engineering Group

Off-Center requests for additional copies of these proceedings should be addressed to the Defense Technical Information Center, Cameron Station, Alexandria, VA 22314-6145. Publications pertinent to the collection of DTIC are, with few exceptions, available to authorized requesters.

Copies of specific articles should be requested from the individual authors.

NAWCWPNS Technical Publication 8242

Published by.....Scientific and Technical Documentation
Collation .....Cover, 84 leaves
First printing.....300 copies

REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704-0188

1. AGENCY USE ONLY *(Leave blank)*	2. REPORT DATE	3. REPORT TYPE AND DATES COVERED
	February 1995	Proceedings

4. TITLE AND SUBTITLE
19th Annual Electronics Manufacturing Seminar Proceedings (U)

5. FUNDING NUMBERS

6. AUTHOR(S)
Various

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
Naval Air Warfare Center Weapons Division
China Lake, CA 93555-6001

8. PERFORMING ORGANIZATION REPORT NUMBER
NAWCWPNS TP 8242

9 SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)
Naval Air Warfare Center Weapons Division
China Lake, CA 93555-6001

10 SPONSORING/MONITORING AGENCY REPORT NUMBER

11. SUPPLEMENTARY NOTES

12A. DISTRIBUTION/AVAILABILITY STATEMENT
A Statement; approved for public release; distribution is unlimited.

12B. DISTRIBUTION CODE

13. ABSTRACT ***(Maximum 200 words)***

(U) Presented are the proceedings of the 19th Annual Electronics Manufacturing Seminar, held on 22–24 February 1995, in Ridgecrest, Calif. The proceedings include the papers presented at the Seminar and cover all aspects of soldering technology and electronics manufacturing. The proceedings are a compilation of information provided by both nongovernment and government sources. The proceedings are published in the interest of furthering communication and broadening awareness of current activities among soldering technology and electronics manufacturing specialists.

14. SUBJECT TERMS
See reverse.

15. NUMBER OF PAGES
163

16. PRICE CODE

10 SECURITY CLASSIFICATION OF REPORT	10 SECURITY CLASSIFICATION OF THIS PAGE	10 SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT
UNCLASSIFIED	UNCLASSIFIED	UNCLASSIFIED	SAR

Alternate cleaning materials
Water-soluble flux
Alternate fluxes for rework and repair
Batch semi-aqueous solvents
Solder joint durability
Ceramic gull wing
Finite element modeling
No-clean soldering process
Lead-free solders
Wetting balance
No-clean fluxes
Wave soldering process improvement
Surface-mount solder reliability
Solder paste in ultra fine pitch era
Certification and training trends

CONTENTS

INTRODUCTION

During 1994, many significant changes occurred within the Department of Defense (DOD). Of great significance is the continued shrinking of defense budgets, which necessitates increased emphasis on acquisition reform. Continued use of MILSPECs and MILSTDs that resulted in the creation of a defense-unique segment of our industrial base has been challenged. Quite simply, DOD cannot afford to pay an increasing defense-unique premium for goods and services. Because of these economic pressures, as well as the need to ensure America's national security, our challenge is to do our part in creating a dual-use industrial base capable of producing military products that meet DOD-unique performance requirements without the costs associated with a separate and distinct defense industry.

The 19th Annual Electronics Manufacturing Seminar affords the opportunity for the electronics industry, defense agencies, and academia to exchange ideas, review emerging technologies, and establish relationships to foster continually increasing cooperative efforts. The synergy resulting from increased cooperation will enable the U.S. to effectively meet the defense challenges of the 21st century.

Environmentally responsible design and manufacturing continue to be extremely important aspects of our industry. However, we must not lose sight of the need for advanced technology insertion, which often results in environmental hazards, to provide our military with clearly superior weaponry. Thus, our challenge is to develop advanced weapon systems within the constraints imposed by declining budgets, environmental responsibility, and acquisition reform.

Manufacturing engineering expertise is needed to continually advance the best practices present in today's industrial base. Productivity, producibility, and quality continue to be the goals we must all pursue. By focusing on these goals, each of us will do our part to ensure that affordable, reliable, and technically superior weapons are available for our troops. Through effective improvement and expansion of the use of the best practices available within the U.S. electronics industrial base, we will be able collectively to meet these goals. The Manufacturing Engineering Division of the Naval Air Warfare Center at China Lake is committed to supporting continual improvement of electronics manufacturing capabilities in the U.S.

We look forward to working together to meet the diverse challenges of maintaining a superior national defense force. We appreciate your involvement in electronics manufacturing and especially thank you for joining us at the 19th Annual Electronics Manufacturing Seminar.

Ray C. Terry, Head
Manufacturing Engineering Division
Systems Engineering Department

ALLOY 42—
A MATERIAL TO BE AVOIDED FOR
SURFACE MOUNT COMPONENT LEADS AND LEAD FRAMES

By

Werner Engelmaier
Engelmaier Associates, Inc.
Mendham, NJ 07945

and

Baldemar Fuentes
Hewlett-Packard Company
Boise, ID 83714-0015

As originally published in the *Surface Mount International Conference Proceedings*, San Jose, Calif., August 1994.

ABSTRACT

Alloy 42, and similarly Kovar, were developed to provide metallic feed-throughs from the interior of ceramic components to the exterior. The low coefficient of thermal expansion (CTE) of ceramic needs to be nearly matched by the feed-through metal to allow reliable hermetically sealed connections. For this purpose these alloys have served very well.

However, because of its wide-spread use for military applications, for which component hermeticity has been required, as well as because of the easier attachment of low-CTE die to low-CTE lead frames, Alloy 42 has found its way into plastic components with often disastrous results.

When surface mount solder joints connect materials with different CTEs, global thermal expansion mismatches result. Also, if the materials to which the solder bonds have CTEs different from the CTE of solder, local thermal expansion mismatches result. These thermal expansion mismatches are the cause of most SM solder joint failures.

Alloy 42 and Kovar not only cause significant global and local thermal expansion mismatches, but are inherently more difficult to solder because of the low solubility of nickel and iron, the main constituents of these alloys, in tin. Pull tests of solder joints show that under the best of circumstances a solder joint that includes a Alloy 42 or Kovar surface is only half as strong as one made to copper surfaces.

INTRODUCTION

The reliability of electronic assemblies depends on the reliability of their individual elements and the reliability of the mechanical thermal, and electrical interfaces (or attachments) between these elements. One of these interface types, surface mount solder attachments, is unique since the solder joints not only provide the electrical interconnections, but are also the sole mechanical attachment of the electronic components to the printed wiring board and often serve critical heat transfer functions as well.

A solder joint in isolation is neither reliable nor unreliable; it becomes so only in the context of the electronic components that are connected via the solder joints to the printed wiring board. The characteristics of these three elements together with the use conditions, the design life, and the acceptable failure probability for the electronic assembly determine the reliability of the surface mount solder attachment.

The solder joints frequently connect materials of highly disparate properties, causing global thermal expansion mismatches[1-5], and are made of a material, solder, that itself has often properties significantly different than the bonding structure materials, causing local thermal expansion mismatches[4,6].

The severity of these thermal expansion mismatches, and thus the severity of the reliability threat, depends on the design parameters of the assembly and the operational use environment. In Table 1 guidelines as to the possible use environments for nine of the more common electronic applications are illustrated[7].

TABLE 1. Realistic Representative Use Environments, Service Lives, and Acceptable Failure Probabilities for Surface Mounted Electronics by Use Categories[7].

USE CATEGORY	WORST-CASE USE ENVIRONMENT					Years of Service	Acceptable Failure Risk, %
	T_{min} °C	T_{max} °C	ΔT [(1)] °C	t_D hrs	Cycles/ year		
1 CONSUMER	0	+60	35	12	365	1-3	~1
2 COMPUTERS	+15	+60	20	2	1460	~5	~0.1
3 TELECOMM	-40	+85	35	12	365	7-20	~0.01
4 COMMERCIAL AIRCRAFT	-55	+95	20	12	365	~20	~0.001
5 INDUSTRIAL& AUTOMOTIVE -PASSENGER COMPARTMENT	-55	+95	20 &40 &60 &80	12 12 12 12	185 100 60 20	~10	~0.1
6 MILITARY GROUND&SHIP	-55	+95	40 &60	12 12	100 265	~5	~0.1
7 SPACE leo	-40	+85	35	1	8760	5-20	~0.001
7 SPACE geo				12	365		
8 MILITARY AVIONICS a	-55	+95	40	2	365	~10	~0.01
8 MILITARY AVIONICS b			60	2	365		
8 MILITARY AVIONICS c			80	2	365		
			&20	1	365		
9 AUTOMOTIVE -UNDER HOOD	-55	+125	60 &100 &140	1 1 2	1000 300 40	~5	~0.1

& = in addition

(1) ΔT represents the maximum temperature swing, but does not include power dissipation effects; for power dissipation calculate ΔT_e.

Early failures of the solder attachments of components with Alloy 42 lead frames and leads during accelerated testing have been previously documented[8-12].

In this paper we are reporting problems created by Alloy 42 leads in actual product.

PRODUCT DESCRIPTION

The effected product is manufactured at Hewlett Packard's Boise facility and is the formatter circuit board which controls laser printer operation. This printed circuit board assembly consists of a FR-4 PCB with a variety of surface mount components solder attached in a no-clean solder reflow process.

The components in question are 44 I/O 50-mil-pitch (1.27 mm) plastic Small Outline Integrated Circuits (SOIC) Read-Only Memory (ROM) 1.10 x 0.50 in (27.9 x 12.7 mm) packages with Gullwing leads. Of the three Japanese manufacturers supplying these components, Vendors A and B chose Alloy 42 for the leadframe and lead material, while Vendor C chose a copper alloy. In all cases, the component leads come plated with 90Sn/10Pb solder which is not fused.

MANUFACTURING PROCESSES

The components are placed into the PCBs, which have been stencil-printed with 60Sn/40Pb no-clean solder paste, as received. The PCBs are processed in panel form. After the no-clean solder reflow process in a 10-zone convection reflow oven (see Fig. 1 for a typical reflow profile), the PCBs undergo a "through-the-connector" test, a bed-of-nails test, and a functional test followed by a visual inspection. A punch process is used to de-panel the PCBs at the end of the production line.

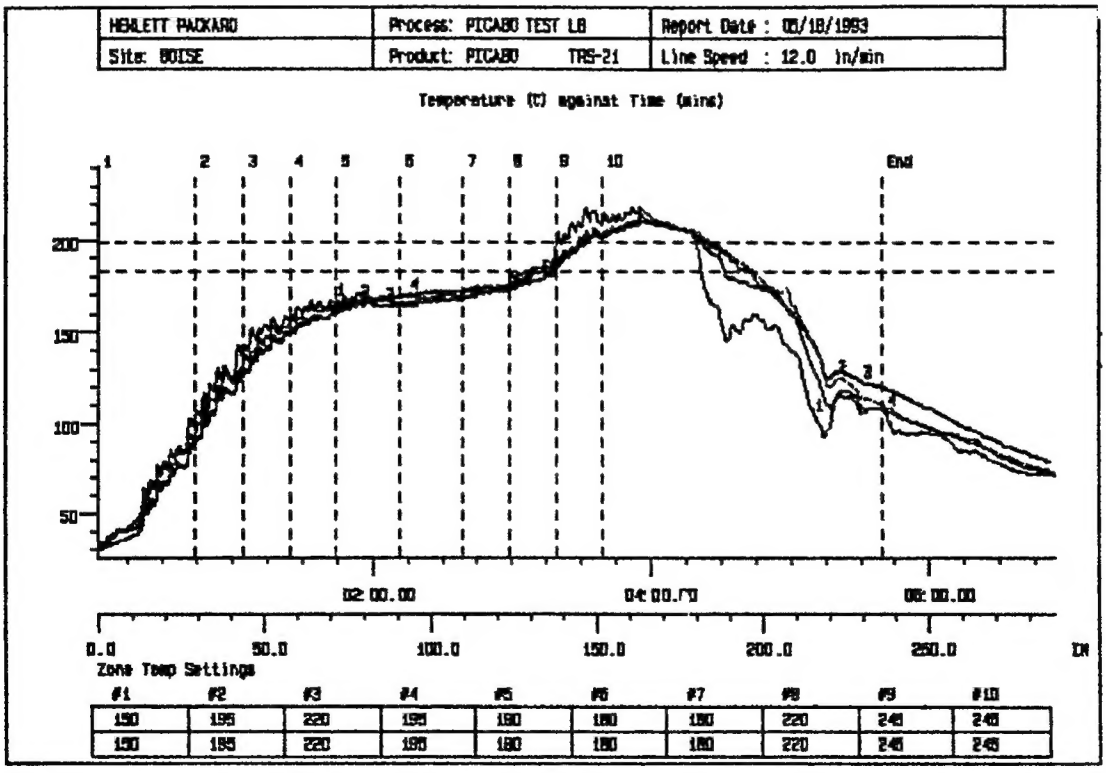


Figure 1 - Typical Solder Reflow Temperature Profile Utilized for the Formatter PCBs.

GLOBAL EXPANSION MISMATCH

Since the SOICs from two vendors contain leadframes consisting of Alloy 42, a substantial mismatch between the coefficients of thermal expansion (CTE) of the SOIC (CTE = 5.2 to 5.9 ppm/°C, depending on the size of the die) and the PCB (CTE = 17±2 ppm/°C) exists. Depending on the thermal use conditions, this CTE-mismatch can result in a significant global thermal expansion mismatch between the SOIC and the PCB. This global expansion mismatch will cyclically stress, and thus fatigue, the solder joints.

It has been experimentally shown[1,13,14] that the fatigue life of surface mount solder joints can be described by a power law similar to the Coffin-Manson low-cycle fatigue equation[15] developed for more typical engineering metals. This equation, subject to some caveats listed later, relates the cyclic visco-plastic strain energy[16], represented by the cyclic fatigue damage term, ΔD, to the mean cyclic fatigue life

$$\overline{N_f} = \frac{1}{2}\left[\frac{2\varepsilon_f'}{\Delta D}\right]^{\frac{1}{c}} \tag{1}$$

where ε_f'=fatigue ductility coefficient, ≈0.325 for eutectic and 60/40 Sn/Pb solder (for other solders the value of ε_f' is expected to be somewhat different).

Solder, uniquely among the commonly used engineering metals, readily creeps and stress-relaxes at normal use temperatures and the rate of creep and stress-relaxation is highly temperature- and stress-level-dependent. Thus, the cyclic fatigue damage term, ΔD, for practical reasons has to be based on the total potential damage at complete creep/stress relaxation of the solder. For cyclic conditions that do not allow sufficient time for complete stress relaxation ΔD is larger than the actual fatigue damage. The temperature- and time-dependent exponent, c, compensates for the incomplete stress relaxation and is given by [5]

$$c = -0.442 - 6\text{x}10^{-4}\overline{T_{SJ}} + 1.74\text{x}10^{-2}\ln\left(1 + \frac{360}{t_D}\right) \tag{2}$$

where $\overline{T}_{SJ}$ is the mean cyclic solder joint temperature and t_D is the half-cycle dwell time in minutes.

While the physical parameters define the mean cyclic fatigue life, solder attachment failures for a group of identical components will follow a distribution —like all fatigue results —which typically is best described by a Weibull statistical distribution[17]. Thus, the fatigue life at any given failure probability can be predicted as long as the slope of the Weibull distribution is known. Thus, the fatigue life of surface mount solder attachments at a given acceptable failure probability, x, is given by

$$N_f(x\%) = \overline{N_f}\left[\frac{\ln(1 - 0.01x)}{\ln(0.5)}\right]^{\frac{1}{\beta}} \tag{3}$$

For solder attachments with leads compliant enough, so that the solder joint stresses are below the yield strength and thus are not bounded by it, the cyclic fatigue damage term is[5]

$$\Delta D(leaded) = \left[\frac{FK_D\,(L_D\,\Delta\alpha\,\Delta T_e)^2}{(133\text{ psi})Ah}\right] \tag{4}$$

where for metric units the scaling coefficient is 919 kPa instead of 133 psi. Equation 4 contains the design parameters that have a first-order influence on the reliability of SM solder attachments. They are

A = effective minimum load bearing solder joint area;
F = empirical "non-ideal" factor indicative idealizing assumptions and accounting for secondary and frequently intractable effects such as cyclic warpage, cyclic transients, non-ideal solder joint geometry, brittle intermetallic compounds, Pb-rich boundary layers, and solder/bonded-material expansion differences, as well as inaccuracies and uncertainties in the parameters in Eqs. 1 through 4; $F \approx 1$ for solder attachments utilizing compliant leads, but is somewhat dependent on the foot length;
h = solder joint height, for leaded attach-ments $h \equiv 1/2$ of solder paste stencil depth as a representative dimension for the average solder thickness;
K_D = "diagonal" flexural stiffness of unconstrained, not soldered, component lead, determined by strain energy methods (see Refs. 18, 19, 20 and 21) or finite element analysis;
$2L_D$ = maximum distance between component solder joints measured from component solder joint pad centers;
N = design life times cyclic frequency, number of operating cycles during product life;
$N_f(x\%)$ = number of operating cycles to $x\%$ failure probability;
T_C, T_S = steady-state operating temperature for component, substrate ($T_C > T_S$ for power dissipation in component) during high temperature dwell;
$T_{C,0}, T_{S,0}$ = steady-state operating temperature for component, substrate during low temperature dwell, for non-operational (power off) half-cycles $T_{C,0} = T_{S,0}$;
$\overline{T_{SJ}}$ = $(1/4)(T_C+T_S+T_{C,0}+T_{S,0})$, mean cyclic solder joint temperature;
α_C, α_S = coefficient of thermal expansion (CTE) for component, substrate;
β = Weibull shape parameter, slope of Weibull probability plot, typically 4 for stiff leadless attachments and 2 for compliant leaded attachments;
ΔD = potential cyclic fatigue damage at complete stress relaxation;
ΔT_C = $T_C - T_{C,0}$, cyclic temperature swing for component;
ΔT_e = $[(\alpha_S \Delta T_S - \alpha_C \Delta T_C)/\Delta\alpha]$, equivalent cyclic temperature swing, accounting for component power dissipation effects as well as component external temperature variations ($\Delta\alpha \neq 0$);
ΔT_S = $T_S - T_{S,0}$, cyclic temperature swing for substrate (at component);
$\Delta\alpha$ = $|\alpha_C - \alpha_S|$, absolute difference in thermal expansion coefficients of component and substrate, CTE-mismatch.

CAVEAT 1 — Solder Joint Quality

The solder joint fatigue behavior and the resulting reliability prediction relationships, Eqs. 1 through 4, were determined from thermal cycling results of solder joints that failed as a result of fracture of the solder, albeit sometimes close to the intermetallic compound (IMC) layers. For solder joints for which layered structures are interposed between the base material and the solder joints, these equations could be optimistic upper bounds if the interposed layered structures become the 'weakest link' in the surface mount solder attachments. Such layered structures could be: metallization layers that have weak bonds to the underlying base material, or are weak themselves, or dissolve essentially completely in the solder; oxide or contamination layers preventing proper metallurgical bond of the solder to the underlying metal; brittle intermetallic compound layers too thick due to too many or improperly long high temperature processing steps.

CAVEAT 2 — Large Temperature Excursions

Solder joints seeing large temperature swings which extend significantly both below and above the temperature region from -20 to +20°C in which the change from stress- to strain-driven solder response takes place, do not follow the damage mechanism described in

Eq. 1[22]. The damage mechanism is different than for more typical use conditions and is likely dependent on a combination of creep-fatigue, causing early microcrack formation, and stress concentrations at these microcracks during the cold temperature excursions, as well as recrystallisation considerations.

CAVEAT 3 — High Frequency/Low Temperatures

For high-frequency applications, $f > 0.5$ Hz or $t_D < 1$ sec, e.g., vibration, and/or low temperature applications, $T_C < 0°C$, for which the stress relaxation and creep in the solder joint is not the dominant mechanism, the direct application of the Coffin-Manson[15] fatigue relationship might be more appropriate. This relationship is

$$\overline{N_f} = \frac{1}{2}\left[\frac{2\varepsilon_f'}{\Delta\gamma_p}\right]^{\frac{1}{c}} \tag{5}$$

where

$\Delta\gamma_p$ = cyclic plastic strain range,
c ≈ -0.6,
β ≈ 3.

CAVEAT 4 — Local CTE Mismatch

For applications for which the global thermal expansion mismatch is very small, e.g. ceramic-on-ceramic or silicone-on-silicone (flip-chip solder joints), the local thermal expansion mismatch becomes the primary cause of fatigue damage. Equation 4 does not address the local thermal expansion mismatch. This reliability problem needs to be assessed using an interfacial stress analysis[23] and appropriate accelerated testing.

For leaded surface mount components with lead materials that have CTEs significantly lower than copper alloy materials, e.g. Kovar or Alloy 42, the results from Eqs. 1 and 4 will be optimistic, since the fatigue damage contributions from the solder/lead material CTE-mismatch, the local thermal expansion mismatch, are not included.

CAVEAT 5 — Very Stiff Leads/Large Expansion Mismatches

Equation 4 assumes that the compliant leads prevent stresses in the solder joints to reach levels where substantial yielding, and thus plastic strains prior to creep and stress relaxation, can take place.

However, for very stiff leads (e.g., SM connector headers), perhaps at lead stiffnesses $K_D > \sim 500$ lb/in (90 N/mm) and/or for very large thermal expansion mismatches (e.g., ceramic multi-chip modules (MCM) on FR-4) resulting in strain ranges $\Delta\gamma > \sim 10\%$, the damage estimates in Eq. 4 can be substantially in error, because this situation is not covered by Eq. 4.

For very stiff leads the stresses calculated in Eq. 4 can exceed the yield strength of the solder. Since yielding will not permit stresses significantly higher than the yield strength, these calculated stress ranges will overestimate the cyclic fatigue damage and thus result in substantially underpredicted fatigue lives. To prevent this analytical error, the stress range in Eq. 4 needs to be bounded by the yield strength in shear.

For very large thermal expansion mismatches the full displacements will not be transmitted to the solder joints; possible exceptions are situations where very stiff leads are present as well, in which case the solder joint reliability is best estimated using Eq. 1 for leadless solder attachments. The strain range that can be accommodated by creep and stress relaxation in the solder joints can be significantly exceeded by the displacements resulting

from very large thermal expansion mismatches and the cyclic fatigue damage would be significantly overestimated.

In general, caution might be indicated in all instances were the predicted life is less than 1000 cycles.

Reliability Estimate for the SOICs

The formatter PCBs in laser printers operate in a rather benign thermal environment. The operating temperatures are estimated at: T_C = 41.1, T_S = 40.3, $T_{C,0}$ =$T_{S,0}$ = 20°C with t_D = 715 min; the lead stiffness at K_D = 70 lb/in.

From these and the previously stated parameters together with Eqs. 1 through 4 we obtain a medium fatigue life of 11,000 cycles-to failure and 1,300 cycles to a failure probability of 1% for the worst choices of the parameters. This represents, for the case where the printer is shut off daily, at least 44 and 5.2 years, respectively, subject to the caveats listed earlier.

LOCAL EXPANSION MISMATCH

Since the SOICs from two vendors contain leads consisting of Alloy 42, a substantial mismatch between the coefficients of thermal expansion (CTE) of the leads (CTE = 5.0 ppm/°C) and the solder (CTE = 25 ppm/°C) exists. Depending on the thermal use conditions, this CTE-mismatch can result in a significant local thermal expansion mismatch between the lead and the solder. This local expansion mismatch will cause cyclic interfacial stresses, and thus fatigue, at the Alloy 42/solder interface.

Suhir[23] has shown that the interfacial stresses resulting form the local expansion mismatch follow

$$\tau \propto L\ (\alpha_{Solder} - \alpha_{Base})(T_{max} - T_{min}) \tag{6}$$

where
L = the wetted length of the solder joint.

Suhir[23] has also shown, that besides substantial shear stresses at the interface between the solder joint and the base material to which it is wetted, even larger peeling stresses occur. Both of these stresses are proportional to the parameters given in Eq. 6.

From Eq. 6 it is quite clear, that for leads consisting of Alloy 42 the wetted length of the solder joint, that is the length of the lead foot should be minimized to reduce interfacial stresses. That, of course, is contrary to the good practice that the foot length should be at least three times the lead width for optimum solder joint quality. However, since in most applications, the local expansion mismatch results in contributory damage to the most important damage caused by the global expansion mismatch, this contraindication can be ignored without suffering catastrophic consequences.

EXPERIENCES WITH TESTS AND PRODUCT

The first indication of a problem with the SOIC solder joints was the detection of an intermittent failure by one of our single image test fixtures used for testing after de-paneling.

Under normal visual inspection, the solder joints looked fine giving the appearance of good wetting of both the leads and the lands on the PCBs. However, with the use of a high powered microscope, a very fine crack could be seen along the heel of one of the corner joints. The crack ran along the outline of the lead (see Figure 2 for a similar, but more

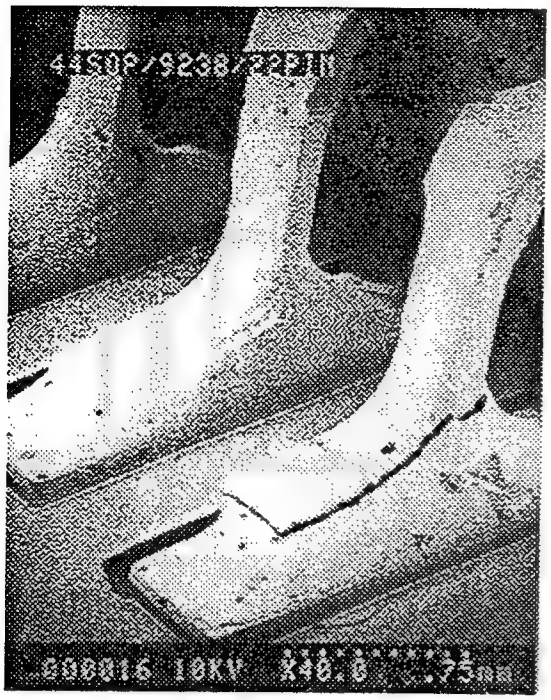


Figure 2 - Photograph of Observed Interfacial Fracture Between Alloy 42 Leads from Vendor A and the Solder.

pronounced crack) and at some points was difficult to distinguish from the edge of the lead.

Upon further inspection, "stress marks" were apparent on the solder joints of other leads of this failed package. These marks appear as hair line ridges near the heal of the joints. These lines are not fractures, but indentions in the solder which, we found, are evidence of severe mechanical stress on the joints. It was also observed, that corner joints were more likely to have these stress marks or fractures.

Source of Stresses on SOIC Solder Joints

In looking for the sources of significant mechanical stresses, we found that in addition to handling in inspection and installation, there are systematic sources of bending stress on our boards during manufacture and testing.

The most significant source of PCB bending is the bed-of-nails testing. The test fixtures induced bending moments primarily along the long axis of the SOICs. The bottom plate of a fixture, containing the spring-loaded contact nails, and the top plate with counteracting push pins, generate forces on the PCBs causing them to bend and twist.

This bending was the immediate cause of the solder joint fractures. Although important, we found that the solution of the problem was not as simple as just eliminating or minimizing the straining of our boards.

Underlying Cause of SOIC Solder Joint Fractures

We found that only the SOICs from Vendor A, one of our three SOIC vendors were showing solder joint fractures.

A number of investigative tests were performed to establish and correct the cause of the different experience with the solder joints of the SOICs from Vendor A.

Dimensional comparisons established that the gullwing leads from Vendor A would tend to have the highest stiffness. The total lead lengths are measured as 1.60, 1.75, and 1.87 mm, respectively for Vendors A, B, and C. Most important for the vertical stiffness of the leads is the length, width, and thick-ness of the leads in the shoulder area, where the leads emerge from the component body. The shoulder length measured 0.38, 0.76, and 0.65 mm for Vendors A, B, and C, respectively, while the corresponding shoulder widths were 0.41, 0.35, and 0.38 mm; the lead thickness was with 0.15 mm the same for all the vendors. Figure 3 illustrates the significant difference in the lead dimensions for Vendors A and B. Thus, the leads from Vendor A had the least favorable of the three vendors for all three of the critical dimensions. The consequence is clearly evident in the vertical lead stiffnesses which have been determined to be K_z = 574, 414, and 332 lb/in, respectively for Vendors A, B, and C and the higher stresses at the lead shoulder for Vendor A in Fig. 3.

The lead material for both Vendors A and B is Alloy 42, while Vendor C it is a copper alloy. Microhardness measurements were made for the leads from Vendors A and B and resulted in 329 HK (32 HRC) and 296 HK (28 HRC), respectively. This indicated that Vendor A utilized workhardened Alloy 42, which is more difficult to solder to than annealed Alloy 42.

The solder joint quality involving Alloy 42 generally suffers from the significantly lower solderability of solder to Alloy 42, because the much lower solubility of nickel and iron, the main constituents of Alloy 42, into tin as compared to copper. In Table 2 the effect on the solder joint quality of the choice of Alloy 42 as the lead material is illustrated. In order to achieve the same good solder joint quality, higher reflow temperatures and a longer time above liquidus temperature are required. However, the inability of some components to withstand higher reflow temperatures makes raising to reflow temperature impossible.

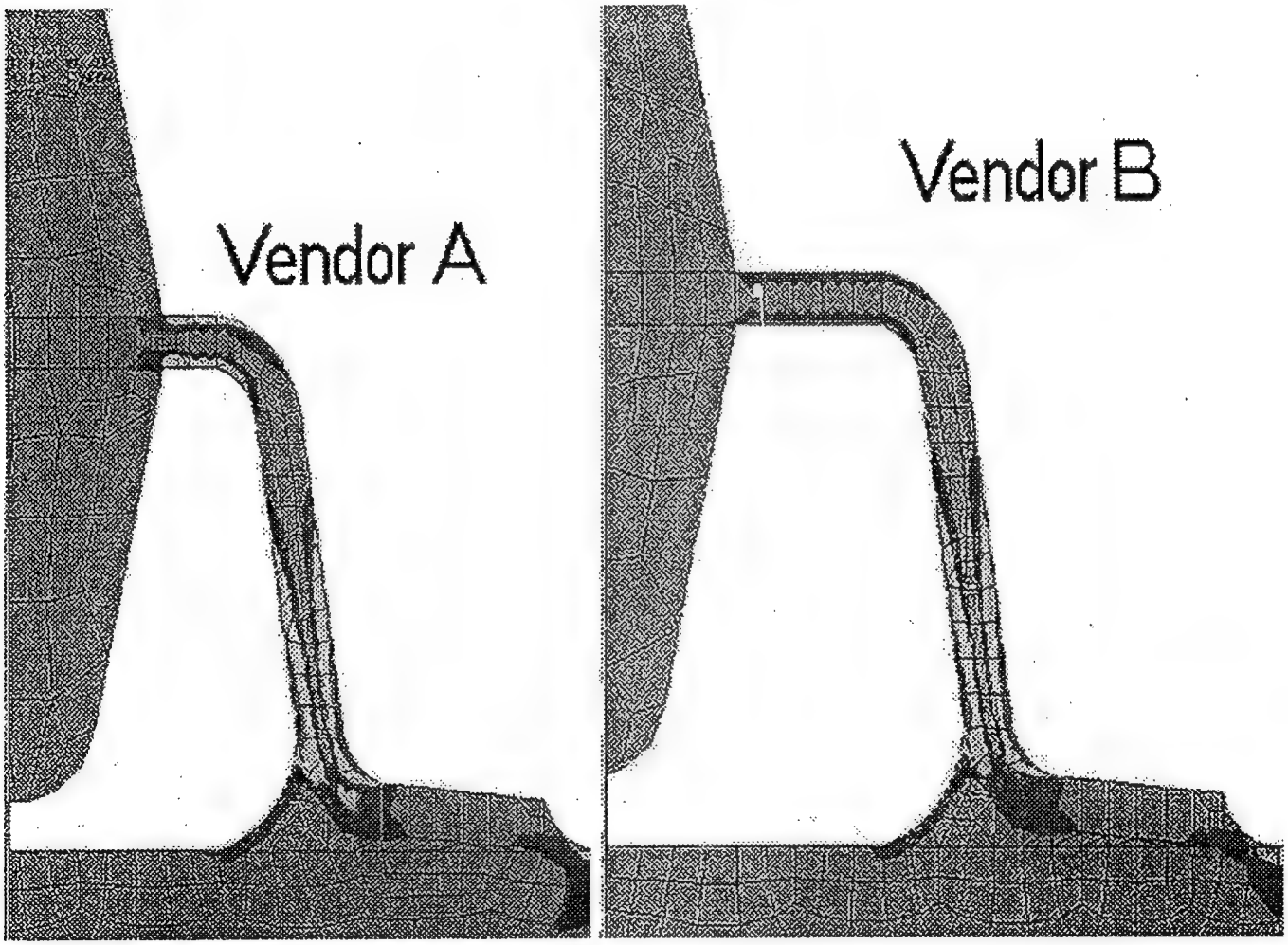


Figure 3 - Finite Element Stress Analysis of Stress Pattern in Gullwing Leads from Vendors A and B Resulting from PCB Bending and Dimensional Comparison.

A common test used to judge the integrity of solder joints is a lead pull test. The body of the component is carefully sawed off at the line where the leads enter the plastic. Then the leads are simply pulled off in the z-direction at a controlled strain rate by a load and displacement sensor.

TABLE 2. Quality of Solder Joints with Copper and Alloy 42 Resulting From Different Reflow Temperatures.

Reflow Temperature °C	Solder Joint Quality	
	60/40 Solder to Copper	60/40 Solder to Alloy 42
~210	just o.k.	marginal to bad
~240	good	just o.k.
~260	good	good

The resulting lower solder joint quality indicated in Table 2 is also clearly evident in Figure 4, where the solder joint pull strength is shown for a variety of differently prepared Alloy 42 and copper leads. Alloy 42 leads, even when etched or pre-reflowed at a higher temperature than can be tolerated by the component, show a substantial reduction in the solder joint pull strength relative to copper. In the worst instance, for the leads of workhardened Alloy 42 from Vendor A, the pull strength is less than half then the pull strength of Vendor C solder joints.

The solder joints with the workhardened Alloy 42 reach the pull strength for the soft Alloy 42 lead from Vendor B only after a 240°C pre-reflow.

The pull strength of 1,000 to 2,000 g/lead apparently results almost entirely from the strength of the solder fillets enveloping the lead foot. The microsection in Figure 5 in Figure 5 shows large sections of the lead/solder interface with gaps between the lead surface and the solder showing an almost total lack of wetting.

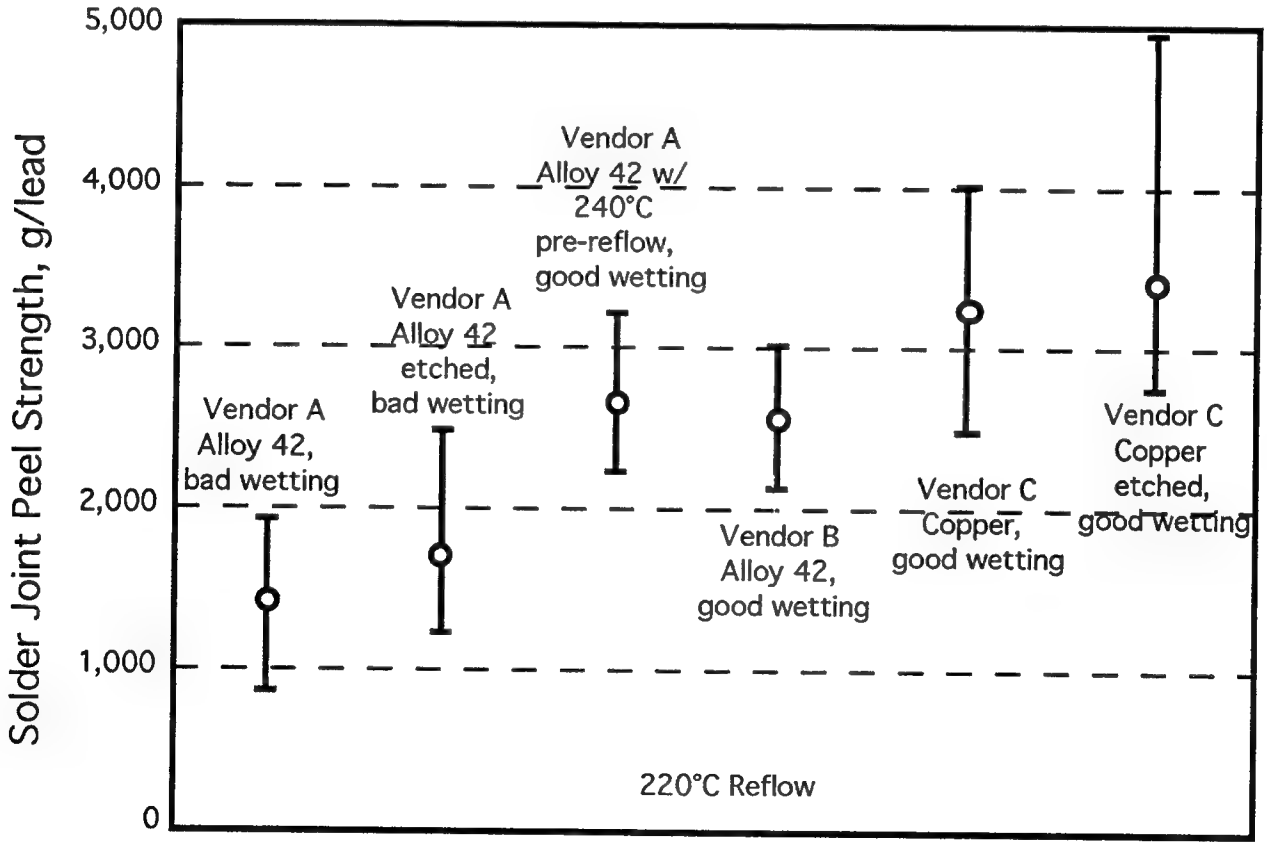


Figure 4 - Solder Joint Pull Strengths for Gullwing Leads Consisting of Alloy 42 and Copper from the Three Vendors.

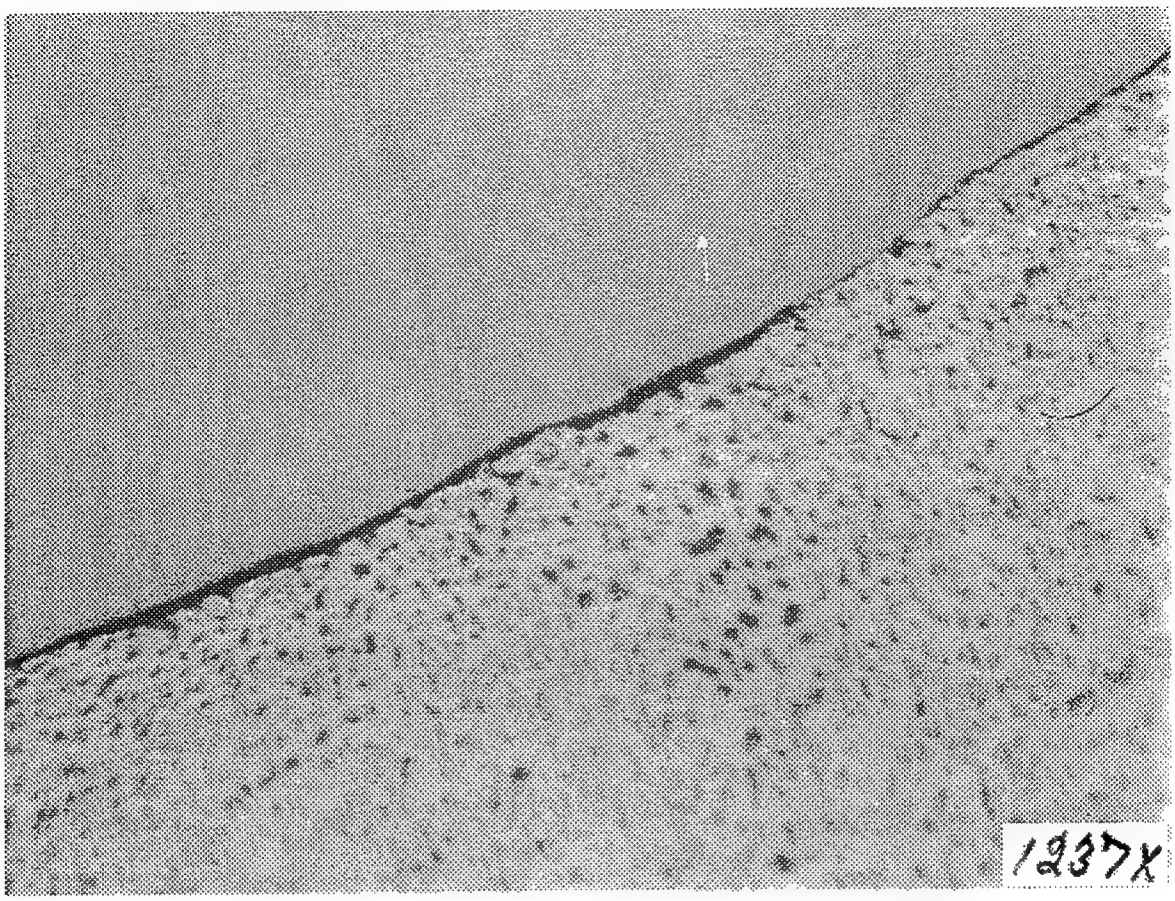


Figure 5 - Microsection of Alloy 42 Gullwing Lead from Vendor A Showing Large Sections of the Lead/Solder Interface with Gaps Between the Lead Surface and the Solder Showing an Almost Total Lack of Wetting.

A special 3-point bending test, with which boards could be flexed known amounts subjecting the SOIC solder joints to fixed strains under repeated cycling, was developed. This test proved to be a good indicator of the differences in solder joint quality. While for SOICs from Vendor A the failures occurred at the solder joint interfaces, deformations of the leads, and even lead fractures at extreme strain levels, resulted for the SOICs from Vendors B and C.

The solder joint fractures from both the product and the tests are always at the lead interface (see Fig. 6) and show no evidence of any intermetallic layer. The majority of the fractures show little solder remaining on the leads.

It is very evident, that these weak solder joints not only cause fractures during processing, but should the solder joints survive manufacture would also pose an increased reliability threat due to thermal stress/ thermal fatigue of solder joints in service.

All the circuit boards with fractured SOIC solder joints were removed from the product population and reworked.

Solutions to SOIC Solder Joint Problem

Significant efforts were made to find a solution to the problem. They included geometric changes of the leads, changes in the lead surface preparation process, and

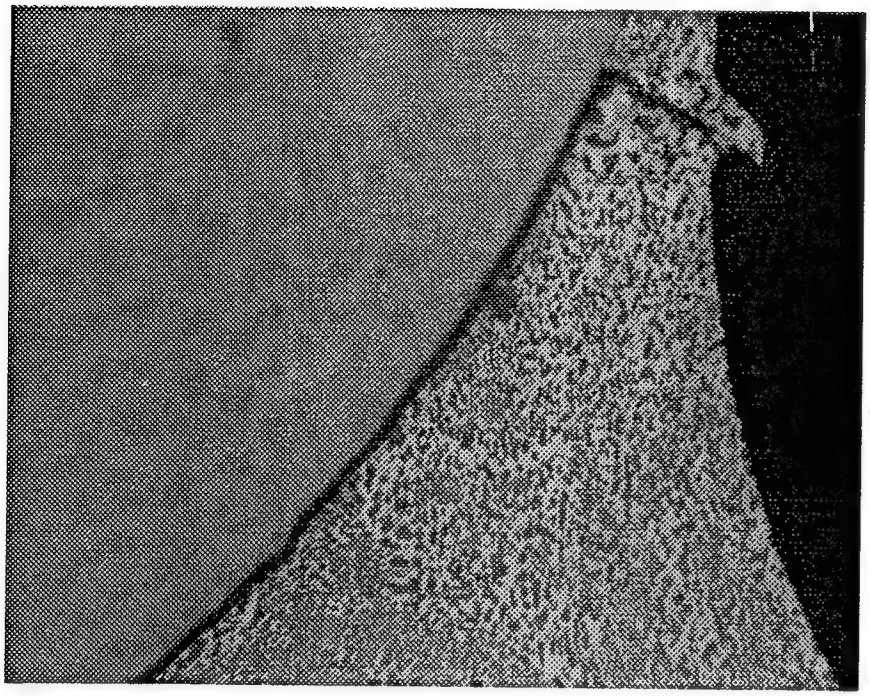


Figure 6 - Microsection of Alloy 42 Gullwing Lead from Vendor A Showing Solder Joint Fractured at the Lead Interface.

changes in the solder plating process. Even in combination, the improvements gained were insufficient. The only adequate solution was a change to a copper alloy lead frame. Vendor A will use copper alloy instead of Alloy 42 for future product.

The bed-of-nails test fixtures have been changed to significantly reduce the stresses on the PCBs during testing.

It is quite clear that there is no need for Alloy 42 in a plastic component. While the die attach to a copper alloy leadframe requires more attention because of the larger difference in the coefficients of thermal expansion of the silicone and the leadframe, it can be accomplished without great difficulties. The higher modulus of elasticity results in somewhat stiffer leads giving the appearance of requiring less care in the handling of the components to prevent accidental lead bending. Utilizing copper alloy lead frames and lead materials would not only result in more consistent and stronger solder joints, but also minimize any thermal expansion mismatches.

SUMMARY AND CONCLUSIONS

A serious problem with fractures of solder joints with Alloy 42 leads occurred with plastic SOICs. The root cause of the problem was identified as the use of workhardened Alloy 42 in combination with a very stiff lead design. Contributory were high bending stresses on the printed circuit board during bed-of-nails testing.

Alloy 42 is inherently more difficult to solder because of the low solubility of nickel and iron in tin. Pull tests of solder joints show that under the best of circumstances a solder joint that includes a Alloy 42 surface is only half as strong as one made to copper surfaces. The workhardened Alloy 42 showed very poor wetting with the solder joint strength in the lead pull test coming primarily from the enveloping solder fillets.

From our experience, it is quite clear that there is no need for Alloy 42 in a plastic component. Utilizing copper alloy lead frames and lead materials would not only result in more consistent and stronger solder joints, but also minimize any thermal expansion mismatches.

ACKNOWLEDGMENTS

We would like to acknowledge the many contributions made by others that are instrumental for this paper. In particular we would like to thank Kristen Gratalo, Ed Davis, Pedro Coca, Marc Nilson, Kevin Brown, Lon Turtle, Paul Dlugosch, Eric Schnieder, and Wade Hezeltine.

(1) Engelmaier, W., "Effects of Power Cycling on Leadless Chip Carrier Mounting Reliability and Technology," Proc. Int. Electronics Packaging Conf. (IEPS), San Diego, CA, November 1982, p. 15.
(2) Engelmaier, W., "Functional Cycles and Surface Mounting Attachment Reliability," Surface Mount Technology, ISHM Technical Monograph Series 6984-002, The International Society for Microelectronics, Silver Spring, MD, 1984, p. 87.
(3) Engelmaier, W., and A. I. Attarwala, "Surface-Mount Attachment Reliability of Clip-Leaded Ceramic Chip Carriers on FR-4 Circuit Boards," IEEE Trans. Components, Hybrids, and Manufacturing Technology, Vol. CHMT-12, No. 2, June 1989, p. 284.
(4) Engelmaier, W., "Performance Considerations: Thermal-Mechanical Effects," in Section 6: Soldering and Mounting Technology, Electronic Materials Handbook, Volume 1, Packaging, ASM International, Materials Park, OH, 1989, p. 740.
(5) Engelmaier, W., "Reliability for Surface Mount Solder Joints: Physics and Statistics of Failure," Proc. Surface Mount Int., Volume 1, San Jose, CA, August 1992, p. 433.
(6) Clech, J-P., F. M. Langerman and J. A. Augis, "Local CTE Mismatch in SM Leaded Packages: A Potential Reliability Concern," Proc. 40th Electronic Components & Technology Conf., Las Vegas, NE, May 1990, p. 377.
(7) "Guidelines for Accelerated Reliability Testing of Surface Mount Solder Attachments," IPC Guidelines IPC-SM-785, The Institute for Interconnecting and Packaging Electronic Circuits, Lincolnwood, IL, November 1992.
(8) Hines, L. L., "SOT-23 Surface Mount Attachment Reliability Study," Proc. 7th Annual Int. Electronics Packaging Conf. (IEPS), Boston, MA, November 1987, pp. 613-629.
(9) Engelmaier, W., "Alloy 42—Not a Choice Material for Surface Mount Leads," 35th Annual IPC Meeting, Bal Harbour, FL, April 1992.
(10) Lau, J. W., S. Golwalkar, S. Erasmus, R. Surratt, and P. Boysan, "Experimental and Analytical Studies of 28-Pin Thin Small Outline Package (TSOP) Solder Joint Reliability," J. Electronic Packaging, Vol. 114, No. 2, June 1992, pp. 169-176.
(11) Noctor, D. M., F. E. Bader, A. P. Viera, P. Boysan, S. Golwalkar, and D. Foehringer, "Attachment Reliability Evaluation and Failure Analysis of Thin Small Outline Packages (TSOPs)," Proc. 43rd Electronic Components and Technology Conf., Orlando, FL, June 2-4, 1993, pp. 54-61.
(12) Noctor, D. M., and J-P. Clech, "Accelerated Testing and Predictive Modeling of the Attachment Reliability of Alloy 42 and Copper Leaded TSOPs," Proc. Nat. Electronic Packaging and Production Conf. (NEPCON East), Boston, MA, June 14-17, 1993, pp. 193-206.
(13) Wild, R. N., "Some Fatigue Properties of Solders and Solder Joints," IBM Tech. Rep. 73Z000421, January 1973.
(14) Solomon, H. D., in Electronic Packaging: Materials and Processes, J. A. Sartell, ed., ASM, 1986, pp. 29-47.
(15) Manson, S.S., Thermal Stress and Low Cycle Fatigue, McGraw-Hill, New York, 1966.
(16) Morrow, J. D., "Cyclic Plastic Strain Energy and Fatigue of Metals," ASTM STP 378, ASTM, Philadelphia, 1964, pp. 45-87.
(17) Engelmaier, W., "IEEE Compliant Lead Task Force--A Progress Report," Proc. 8th Annual Int. Electronics Packaging Conf. (IEPS), Dallas, TX, November 1988, p. 891.
(18) Kotlowitz, R. W., "Comparative Compliance of Representative Lead Designs for Surface Mounted Components," Proc. Int. Electronics Packaging Conf. (IEPS), Dallas, TX, November 1988, p. 908; also in IEEE Trans. Components, Hybrids, and Manufacturing Technology, Vol. CHMT-12, No. 4, December 1989, p. 431.
(19) Kotlowitz, R. W., "Compliance of Surface Mount Component Lead Designs with Rectangular and Circular Cross-Sections," Proc. Int. Electronics Packaging Conf. (IEPS), San Diego, CA, September 1989, p. 1071.
(20) Kotlowitz, R. W., "Compliance Metrics for Surface Mount Component Lead Design, With Application to Clip-Leads," Proc. Surface Mount Components and Technology Conf.

(SMTCON), Atlantic City, NJ, April 1991, p. 1.
(21) Kotlowitz, R. W., and L. R. Taylor, "Compliance Metrics for the Inclined Gull-Wing, Spider J-Bend, and Spider Gull-Wing Lead Designs for Surface Mount Components," Proc. 41st Electronic Components & Technology Conf., Atlanta, GA, May 1991.
(22) Wild, R. N., "1974 IRAD Study - Fatigue Properties of Solder Joints," IBM Report No. M45-74-002, Contract No. IBM 4A69, Jan. 5. 1975.
(23) Suhir, E., "Axisymmetric Elastic Deformation of a Finite Circular Cylinder with Application to Low Temperature Strains and Stresses in Solder Joints," J. Appl. Mech., Vol. 56, No. 2, June 1989, pp. 328-333.

Werner Engelmaier is president of Engelmaier Associates, Inc., and Senior Research Scientist at the CALCE Center for Electronics Packaging at the University of Maryland. Engelmaier Associates, Inc., provides consulting services on reliability, manufacturing, and processing aspects of electronic packaging. This consulting company provides services to OEMs, printed circuit board manufacturers, PWB subcontract assembly companies, and end users, such as telecommunications and computer companies and the military, in the areas of design for reliability, accelerated reliability testing, reliability prediction, design for manufacturability and quality, processing effects, and environmental stress screening for solder joints, plated-through holes, and dynamically used flexible circuitry.

He was on the technical staff of AT&T Bell Laboratories, Whippany, New Jersey, before forming his own company in 1990. During his 24 years at the Bell Labs, he dealt with many aspects involved in electronic packaging and interconnection technology. His efforts ranged from R&D at Bell Labs to "fire fighting" at Western Electric, and included development of specifications and guidelines for products, as well as the technology transfer to production facilities.

He is the author of over 100 technical publications in a variety of fields related to electronic packaging and interconnection technology and has been awarded a number of patents in these areas. He has conducted numerous tutorial workshops for NEPCON, IEPS, IPC, ISHM, and SMTCON. His clients include many computer and telecommunication manufacturers and defense contractors in the U.S. and overseas.

He is active in the American Society for Testing and Materials (ASTM), the Institute of Electrical and Electronics Engineers (IEEE) ECC Computer Packaging Society, the International Electronics Packaging Society (IEPS), and IPC, and has contributed to numerous task forces, specifications, standards, and design guides. He is on the Editorial Advisory Board of *Electronic Packaging & Production* magazine, and chairs committees at IPC and ASTM.

He has been the recipient of many honors and awards, including Best Paper Awards at the IEEE ECC Conference in 1971, the IEPS Conference in 1990, and the Surface Mount International in 1991; the Distinguished Technical Staff Award from AT&T Bell Laboratories in 1986; the Electronic Packaging Achievement Award, jointly awarded from IEPS and *Electronic Packaging & Production* magazine, in 1987; and the IPC President's Award in 1988. For two of his developments, he received R&D 100 Awards in 1978 and 1981 from *Research & Development* magazine.

He was born in Vienna, Austria, and holds degrees in mechanical engineering from Technologisches Gewerbe-Museum (TGM), Vienna, the University of South Carolina, and Massachusetts Institute of Technology. He is a member of the American Society of Mechanical Engineers (ASME), ASTM, the Components, Hybrids, and Manufacturing Technology Society (CHMT) of IEEE, the Institute for Interconnecting and Packaging Electronic Circuits (IPS), IEPS, the Surface Mount Technology Association (SMTA), Phi Beta Kappa, Pi Mu Epsilon, Sigma Xi, and Tau Beta Pi.

Address: Engelmaier Associates, Inc.
23 Gunther Street
Mendham, NJ 07945

Baldemar Fuentes is a Materials Engineer/ Manufacturing Development Engineer for Hewlett-Packard with more than 4 years' experience in design, materials, and manufacturing.

He has a bachelor of science and a master of science degree in mechanical engineering from the Massachusetts Institute of Technology.

Address: Hewlett-Packard
11311 Chinden Blvd.
Boise, ID 83714-1023

Conformal Coating Adhesion Over No-Clean Fluxes

by

Tim Crawford
Project Leader
Electronics Manufacturing Productivity Facility
Indianapolis, Indiana

ABSTRACT

The impending phaseout of chlorofluorocarbon-based solvents has spawned a new generation of fluxes called "low residue," or "no-clean." These fluxes are designed to leave little or no residues upon completion of the soldering process. Any residue left is benign and should not degrade the reliability of the printed wiring assemblies (PWA). One concern with these residues, however, is with the adhesion of the protective conformal coating that is sometimes applied to the PWA to protect it from harsh environmental conditions. In a three-phase effort, the Electronics Manufacturing Productivity Facility (EMPF) evaluated the adhesion and performance of traditional and low volatile organic compound (VOC) conformal coatings when applied over test coupons and mixed technology PWAs manufactured with low residue fluxes and pastes. This study evaluated conformal coating adhesion to common printed circuit materials such as bare copper, hot air solder leveled (HASL), photoimageable (PI) solder mask, and dry film solder mask when processed with low residue fluxes. Test coupons were environmentally stressed and compared to coupons processed with a control group containing no flux and paste residues. This paper outlines the research.

INTRODUCTION

Unprotected printed wiring assemblies (PWAs) are susceptible to damage from various sources of contamination and environmental conditions. Contamination derived before, during and after the manufacturing process, coupled with harsh environmental conditions, can lead to corrosion and electrical failure over time. To protect the PWA in the field, the circuit board industry will typically apply a protective barrier known as a conformal coating. To properly adhere to the PWA and provide a good seal, the conformal coating must be applied to a clean, dry surface. Improper adhesion can jeopardize the reliability of the PWA.

The impending phaseout of chlorofluorocarbon-based solvents has spawned a new generation of fluxes called "low residue," or "no-clean." These fluxes are designed to leave little or no residues upon completion of the soldering process. Any residue left is benign and

should not degrade the reliability of the PWA. One concern with these benign residues is with the adhesion of the protective conformal coating to the PWA. The Electronics Manufacturing Productivity Facility (EMPF) evaluated the adhesion and performance of polyurethane, acrylic, silicone, and paraxylylene conformal coatings when applied over test coupons manufactured with low residue fluxes and pastes using nitrogen atmosphere soldering and reflow.

METHODOLOGY

Phase 1 evaluated 11 low residue fluxes and 12 low residue pastes for their influence on the adhesion of traditional conformal coatings. Test coupons containing FR4, copper, hot air solder leveled (HASL), photoimageable, and dry-film mask were processed with various low residue pastes and fluxes. The coupons were then coated and subjected to environmental stress screening (ESS) before being subjected to ASTM method D3359 adhesion testing.

Phase 2 selected 14 low volatile organic compound (VOC) conformal coatings from five families (acrylic, silicone, urethane, epoxy, and paraxylylene), and evaluated their ability to adhere to test coupons processed with traditional fluxes that had been cleaned. The same test coupon design, ESS tests, and adhesion test used in Phase 1 were performed.

Phase 3 selected one low VOC conformal coating from each family from Phase 2, and applied them to mixed technology PWAs that had been processed with selected low residue fluxes and pastes selected from Phase 1. The assemblies were tested for both topside and bottomside adhesion as well as surface insulation resistance (SIR).

PHASE 1

To evaluate every manufacturer of every flux along with every manufacturer of every conformal coating would be impossible. Since this was primarily a flux study, we decided to conduct an informal industry survey and select one acrylic, polyurethane, silicone and paraxylylene to represent their respective families. Specialty Coating Services of Indianapolis, Indiana volunteered to apply the coatings to the test coupons.

The flux and paste selection was more complicated. Unlike the "good old" rosin flux that had a relatively straight-forward chemistry and was rated by its activity, the definition of no-clean is somewhat broad. The long list of materials was abbreviated by grouping the materials into resin, rosin, or rosin/resin free categories. The groups were further broken down by solids content, activator, and carrier. Twelve pastes and eleven fluxes were chosen from these groups to provide a good representation of the no-clean industry.

The liquid fluxes were applied to the test coupons using a high pressure spray system designed for use with no-clean fluxes. Precision Dispensing Equipment of Bay Village, Ohio, volunteered to bring the system to the EMPF, set up, and operate the equipment on an as-needed basis. The fluxes were applied to the coupons at two different thicknesses to

determine if flux quantity influenced conformal coating adhesion. The test coupons were then processed on a nitrogen inerted wave soldering machine using a profile recommended by the material vendor.

The no-clean solder pastes were applied to the metalized areas of the test coupons using an 80-mesh, 10-mil-thick screen. The pastes were also reflowed in a nitrogen environment using forced convective air reflow and a profile recommended by the material vendor.

The test coupon was made of FR4 material, measured 4.00 inches by 5.00 inches by 0.0062 inches (10.20 x 12.75 x 0.024 cm) and was routed so that it could be easily snapped into 4 equal pieces (see Figure 1). Each piece contained a 1.00 inch by 1.50 inch (2.54 x 3.80 cm) copper rectangle with a 0.50 inch by 1.00 inch (1.27 x 2.54 cm) solder mask strip down the center. Two different types of solder masks were used: photoimageable and dry film. In addition, some test coupons were solder leveled to give a tin/lead surface over the bare copper. The two masks and the two metal surfaces were mixed and matched to give the following four test coupon combinations:

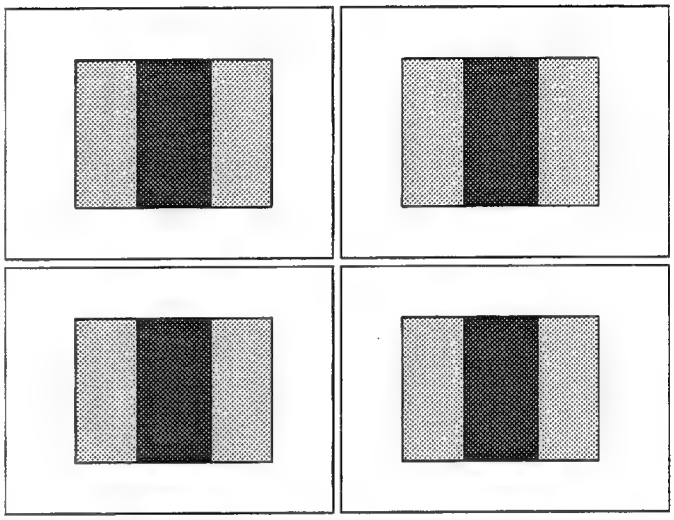


FIGURE 1 Test Coupon For Phases 1 & 2

- Copper/Photoimageable
- Copper/Dry Film
- HASL/Photoimageable
- HASL/Dry Film

Including the FR4, this arrangement gave us the ability to evaluate adhesion of the different conformal coatings to five different substrates and interfaces when contaminated with the various no-clean flux residues. A control group was set aside to evaluate conformal coating adhesion to coupons not contaminated with no-clean flux residues.

Once the conformal coatings were applied and properly cured, representative pieces of the coupons were visually examined and tested for adhesion. The rest of the samples were subjected to ESS. Coupon pieces were subjected to either temperature/humidity, thermal cycle, thermal shock, salt/fog, all tests, or a combination humidity/thermal cycle/thermal shock.

A slightly modified version of ASTM D3359 tape adhesion test was used to measure the adhesion of the various conformal coatings. The ASTM method specifies using a handheld

tool with multiple sharp blades to cut through the coating (see Figure 2). The coupon is rotated 90 degrees and cut again to form a lattice pattern. A specified tape is pressed over the area and removed. The adhesion is rated for each substrate using the following system:

0 Flaking and detachment worse than grade 1.

1 The coating has flaked along the edges of cuts in large ribbons and whole squares have detached. The area affected is 35-65% of the lattice.

2 The coating has flaked along the edges and on parts of the squares. The area affected is 15-35% of the lattice.

3 Small flakes of the coating are detached along the edges and at the intersections of cuts. The area affected is 5 -15% of the lattice.

4 Small flakes of the coating are detached at intersections; less than 5% of the area is affected.

5 The edges of the cuts are completely smooth; none of the squares are detached.

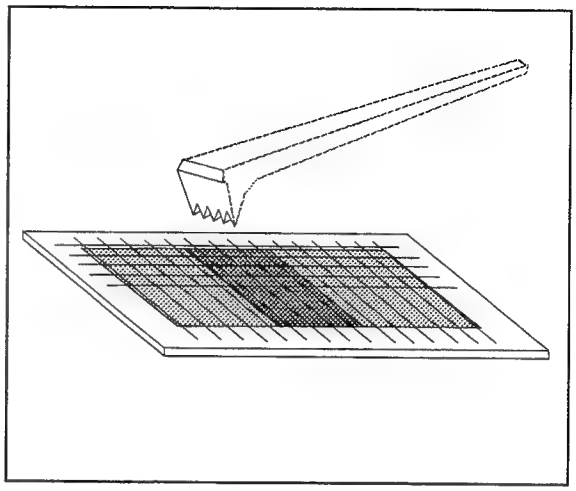


FIGURE 2 Crosshatch Testing

To eliminate as much of the subjectivity as possible, the tool was not handheld, as specified in ASTM D3359. Instead, an IBM robot was fitted to hold the cutting tool and test coupon and programmed to perform the actual cutting. This gave uniform depth, pressure, and lattice formations throughout the evaluation. In addition, the same technician was used to perform all of the tape applications and ratings.

The adhesion for each substrate was rated on the 0-5 scale then converted to a percent rating. This was necessary because not all materials had the same amount of coupons. In addition, coupons may have been processed improperly due to human or machine error. For example, in a sample of four different coupons, if one coupon is lost (HASL/photoimageable), of the remaining three coupons, all have FR4, two have copper, one has HASL, two have dry film mask, and one has photoimageable. If all the three coupons have perfect adhesion to all materials the rating would be as follows:

RATING		MATERIAL
15	(3 X 5)	**FR4**
10	(2 X 5)	**COPPER**
5	(1 X 5)	**HASL**
5	(1 X 5)	**PHOTOIMAGEABLE MASK**
10	(2 X 5)	**DRY FILM MASK**

In this simplified example, one could mistakenly conclude that this coating adhered best to the FR4, but not very well to the HASL or the photoimageable mask.

The data was graphed and analyzed four different ways. The first way (Figure 3) shows the overall adhesion by ESS test of one coating to all of the substrates when contaminated with one particular flux or paste residue. In the second way (Figure 4), the same data is graphed so each substrate rating is plotted side-by-side so that one could more easily see the impact on the individual substrates. In the example, photoimageable mask and FR4 seemed to be the least effected by the ESS, while copper appeared to be the most effected. We can also see that multiple stress tests are most degrading to the copper. The third (Figure 5) way of graphing the data showed how all of the paste performed after each ESS test for each particular coating. In the example, pastes F and L held up the best for the humidity/thermal cycle/thermal shock/salt-fog test. The fourth graph (not shown), is similar to the second graph and showed side-by-side how each substrate reacted for each residue during each ESS test.

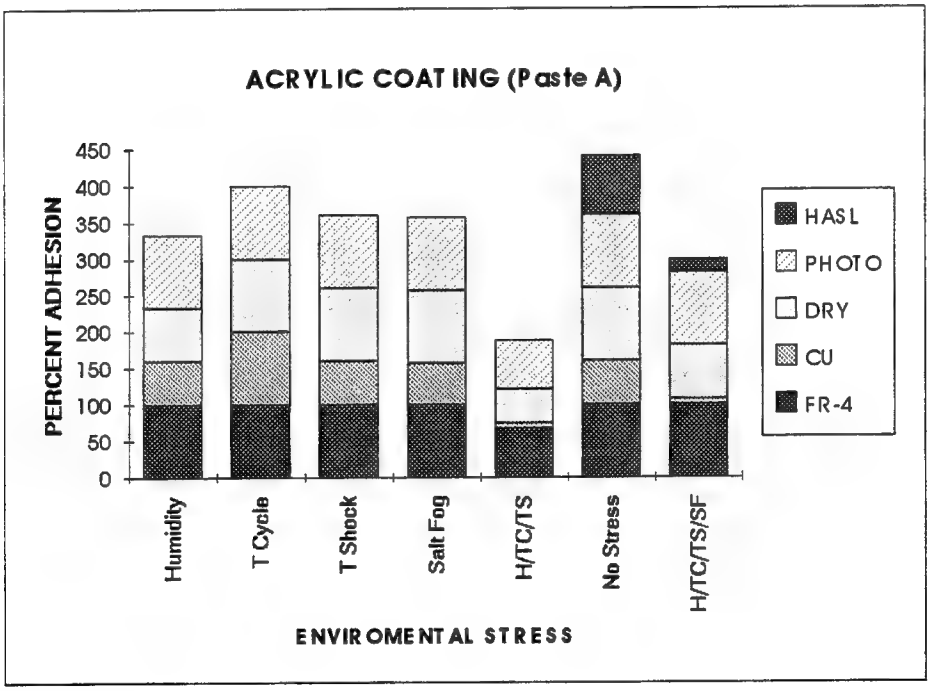


FIGURE 3 Acrylic vs Flux vs ESS

PHASE 2

Phase 2 tested 14 low VOC conformal coatings from five families (acrylic, silicone, urethane, epoxy and paraxylylene) and evaluated their ability to adhere to test coupons manufactured with traditional fluxes that had been cleaned. The same test coupon design, ESS tests, and adhesion test used in Phase 1 were performed.

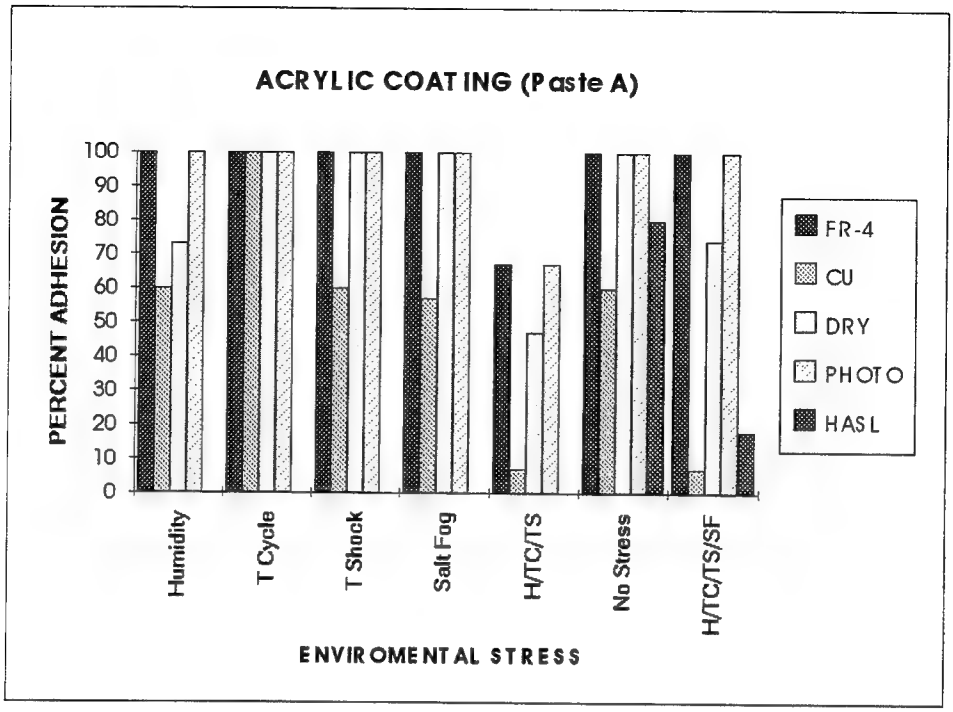


FIGURE 4 Coating vs Paste vs ESS Graphed Side-By-Side

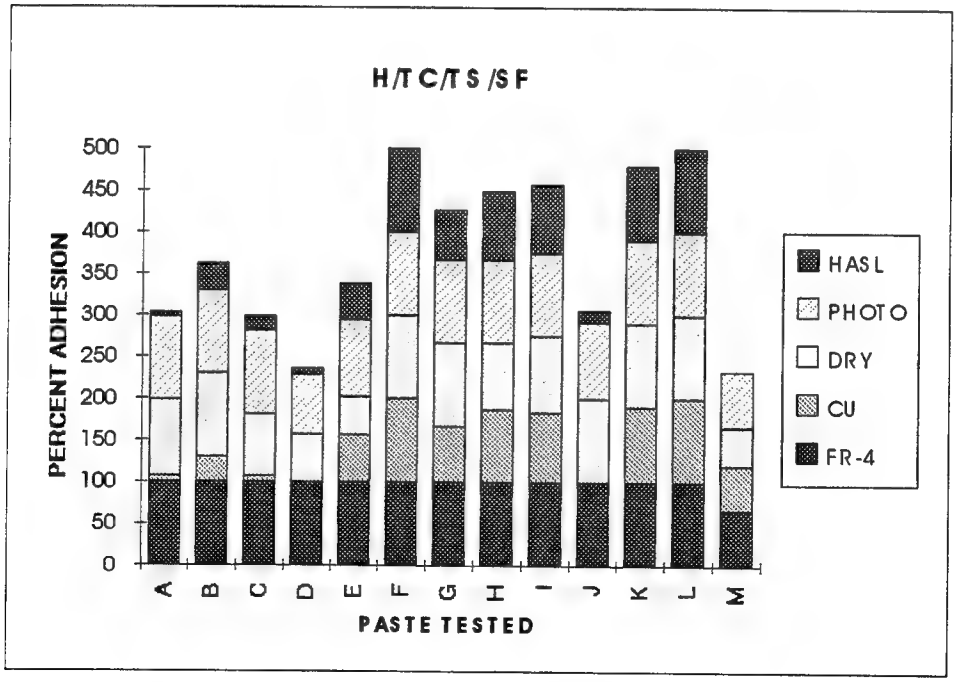


FIGURE 5 All Pastes vs Materials for Complete ESS

Both the water soluble and rosin fluxes were applied to the test coupons using a manually controlled spray bottle. The assemblies processed with water soluble flux were cleaned in the Electronics Controls Design Model 6300 Aqueous Batch Cleaner using a 150°F deionized water wash for 10 minutes followed by 3, 1-minute rinses. The assemblies manufactured with rosin flux used the same cleaning machine but washed with a 10% concentration of Armakleen Solvent E-2001 for 3 minutes at a temperature of 150°F. The wash was followed by 3, 1-minute rinses with deionized water.

Again, the conformal coatings were applied by SCS using the thickness, process, and curing procedures recommended by the manufacturer. The coupons were then brought back to the EMPF for ESS and adhesion testing.

PHASE 3

The low-residue fluxes and pastes that were used in this phase of the project are listed in Table 2. Considering the adhesion test results only, these fluxes and pastes performed the best when used with traditional conformal coatings on our test coupons. In addition, two groups using RMA or water soluble paste and flux combinations were cleaned and used as control groups to represent current industry conditions.

TABLE 2 Flux & Paste Selection

	PASTE	FLUX
Control:	Alpha RMA 209 Amtech WS-465XT	Alpha 615 RMA Lonco Organo Flux 3355 VF Water Soluble
Low-residue:	AIM LR5 AIM Base I	Alpha 970S Kester 970S Hi-Grade 3570-T Alpha NR200

The low VOC conformal coatings are listed in Table 3. Considering the adhesion test results only, these conformal coatings performed the best when used with traditionally fluxed and cleaned test coupons.

TABLE 3 Conformal Coating Selection

Acrylic:	Quick Cure 576
Urethane:	Dymax 986
Epoxy:	Envibar 1244T
Silicone:	Loctite 5290
Parylene:	Parylene C

The test vehicle for Phase 3 was a mixed technology PWA made of FR4 material and measured 6.00 inches by 5.00 inches by 0.062 inches (2.4 x 2.0 x 0.024 cm) (see Figure 6). The solder mask used was a liquid photoimageable mask that met IPC-SM-840B Class 3 and Bellcore specifications. Only half of the board was populated to better compare the influence of components. The four comb patterns used for SIR measurements

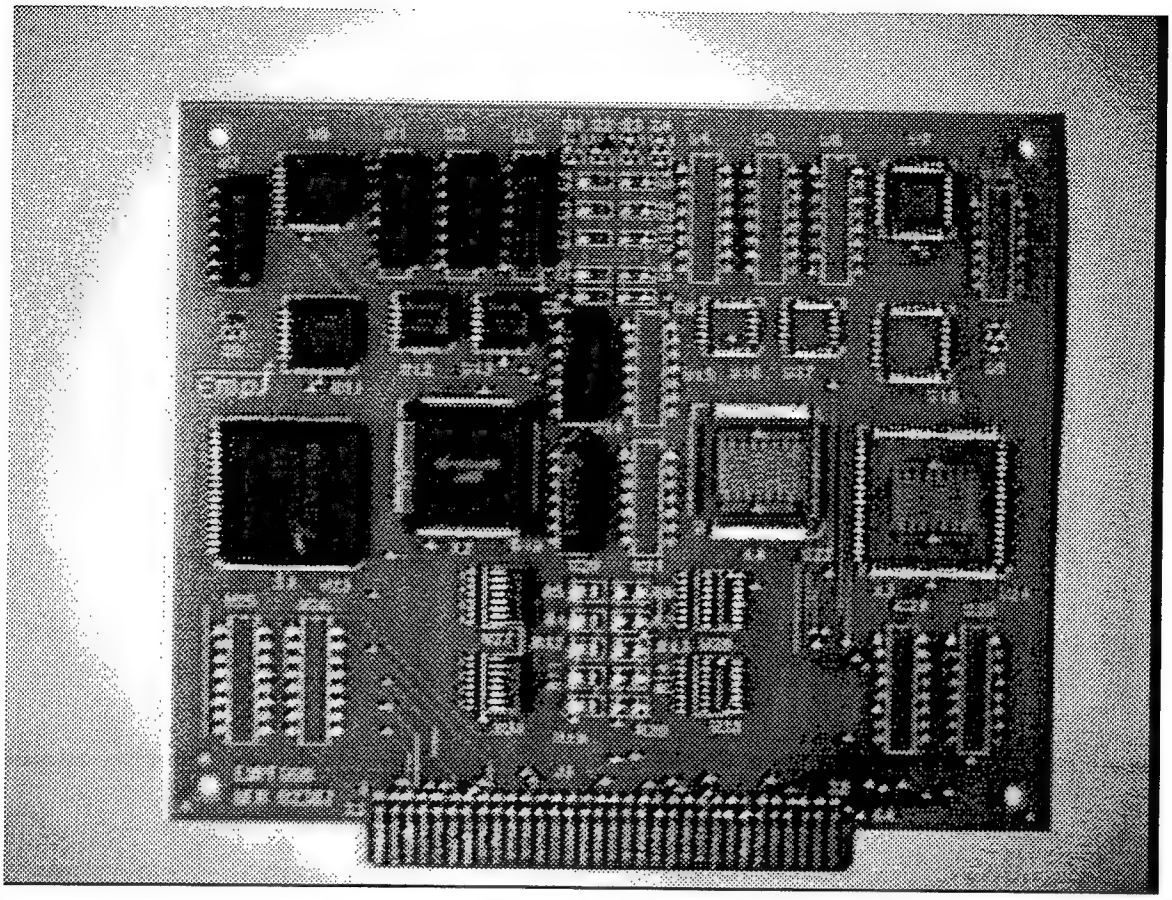


FIGURE 6 EMPF 008 Test Assembly

were located on the topside of the board. Two of the patterns were positioned under surface mount components and two were left uncovered.

Conclusions

Unfortunately, this paper was due before all of the data for Phase 3 was analyzed and conclusions could be drawn. All laboratory testing, ESS, SIR, and adhesion testing is complete, and the data will be presented at the conference. A full report should be available from the EMPF library by first quarter of 1995.

Tim Crawford is a Project Leader for the Electronics Manufacturing Productivity Facility (EMPF) with more than 9 years' experience in various aspects of the manufacturing process, focusing primarily on cleaning and cleanliness testing.

A member of IPC, he is vice-chairman of the Acoustic Energy Cleaning Task Group and co-chairman of the Ionic Cleanliness Testing Task Group. He received the EPA Stratospheric Ozone Protection Award in 1993.

He has an A.A. degree from Cerro Coso College, Ridgecrest, California.

Address: Electronics Manufacturing Productivity Facility
714 N. Senate Avenue
Indianapolis, IN 46202

A Rigid-flex Backplane for the International Space Station Alpha: A Soldering Challenge Solved by a Unique Process

by

Chris Alter, Principal Manufacturing Engineer,
Honeywell Inc., Satellite Systems Operation (SSO), Glendale, Arizona

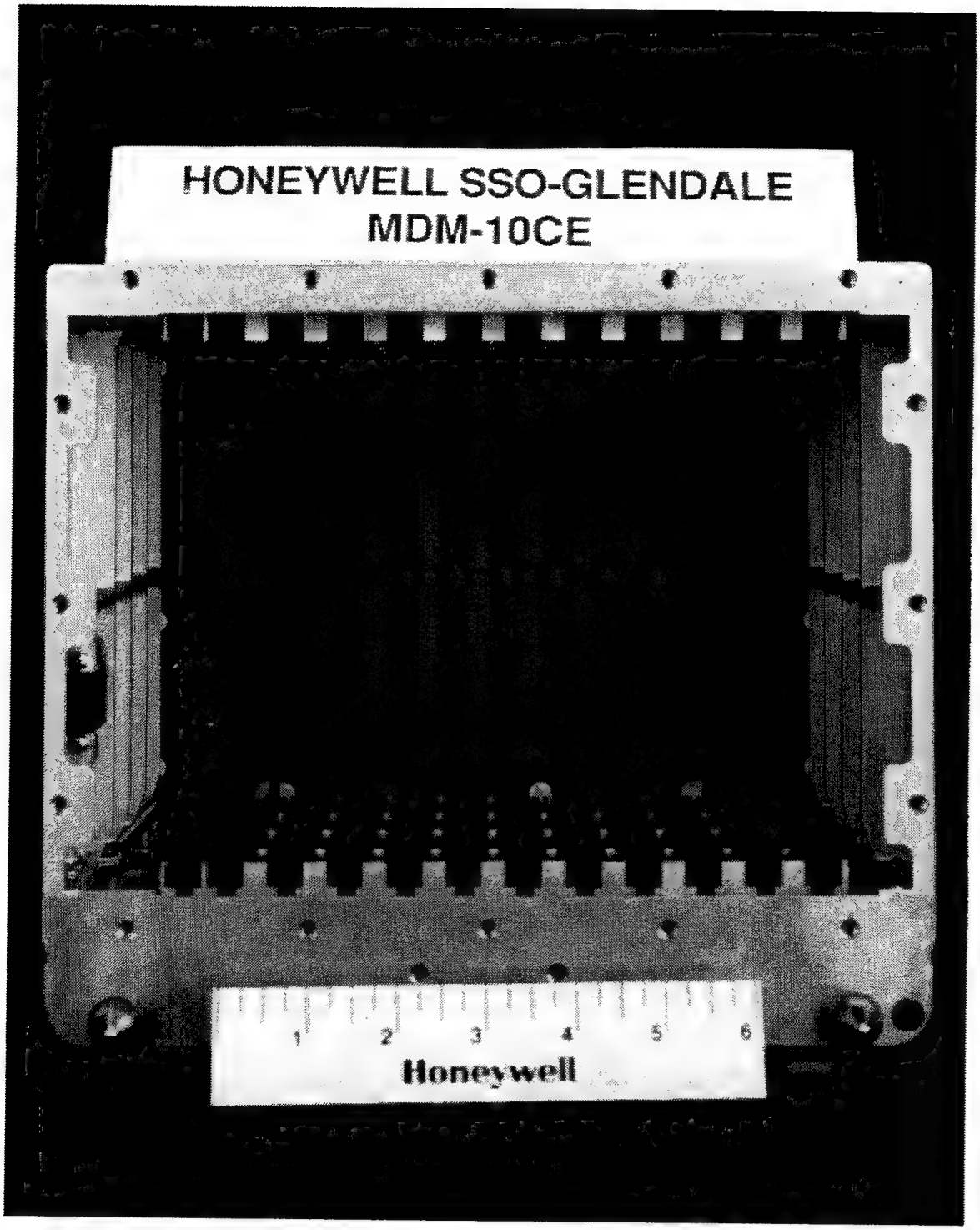
Joe Naperkowski, Principal Manufacturing Engineer,
Honeywell Inc., Satellite Systems Operation (SSO), Glendale, Arizona

ABSTRACT

The National Aeronautics and Space Administration (NASA) International Space Station Alpha (ISSA) uses a distributed architecture Data Management System (DMS) based on a programmable Multiplexer/Demultiplexer (MDM) unit. The DMS contains one primary network, a Fiber-optic Distributed Data Interface (FDDI) for ISSA based systems, and one network dedicated to payloads. The two networks are bridged, allowing the data handling process to occur between payloads and the Space Station without bus contention problems. A key element of MDMs provided by SSO is the motherboard backplane in each unit. The motherboard is a 27 layer rigid flex, 0.170 in. thick and about 11.5 in. by 14 in. The rigid flex connects circuit cards with a large Orbital Replaceable Unit (ORU) connector. The ORU is a monolithic connector with over 4600 connections. Its design was driven by the need to make replacement of externally mounted MDMs easier for astronauts. The thermal mass of the ORU connector and the copper layers in the rigid-flex proved to be a challenge to solder while achieving acceptable top side solder fillets. This paper will address the methods used to develop pre-heat requirements, flux application, flow solder parameters, and top side solder verification. The process development began in the fourth quarter of 1993 and continues today.

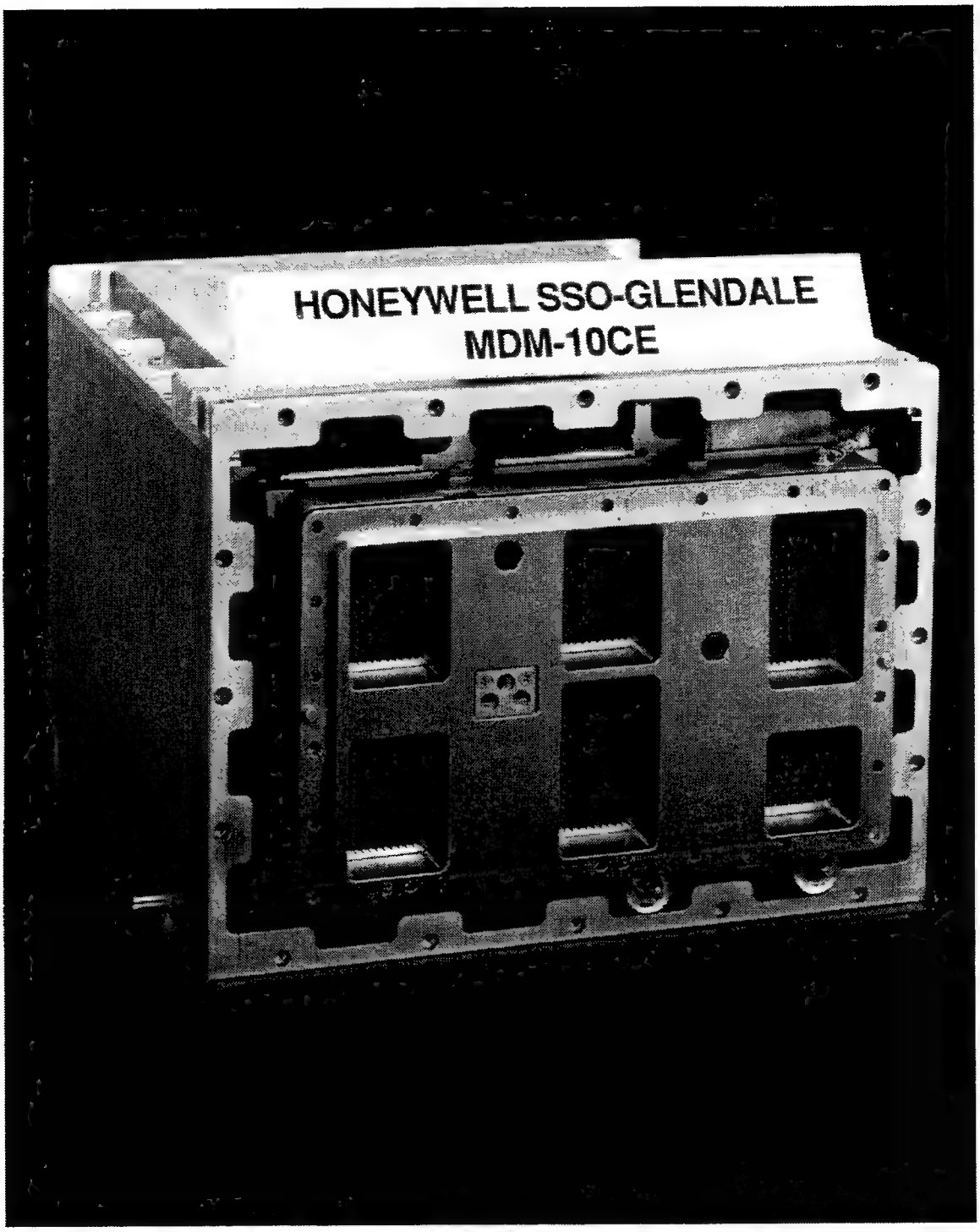
INTRODUCTION

Honeywell SSO knows how to manufacture unique designs. Our production engineers routinely handle complex mechanisms for deep space probes and manned flight electronics. The design of the ISSA is no exception. It uses a complex backplane used to connect ISSA systems and experiments with the station data bus. The backplane is a twenty seven layer rigid flex printed motherboard (Figure 1). This rigid flex board connects the bus multiplex and demultiplex surface mount circuit cards with the ORU Connector (Figure 2). ISSA uses three sizes of MDM modules providing 4, 10, or 16 user configurable Circuit Card Assembly (CCA) slots. Figure 3 shows the MDM-IOCE 10 slot Multiplexer/Demultiplexer. The MDM's are named -4CE, -10CE, and -16CE and are progressively larger versions of the same design. Table 1 lists their physical features.



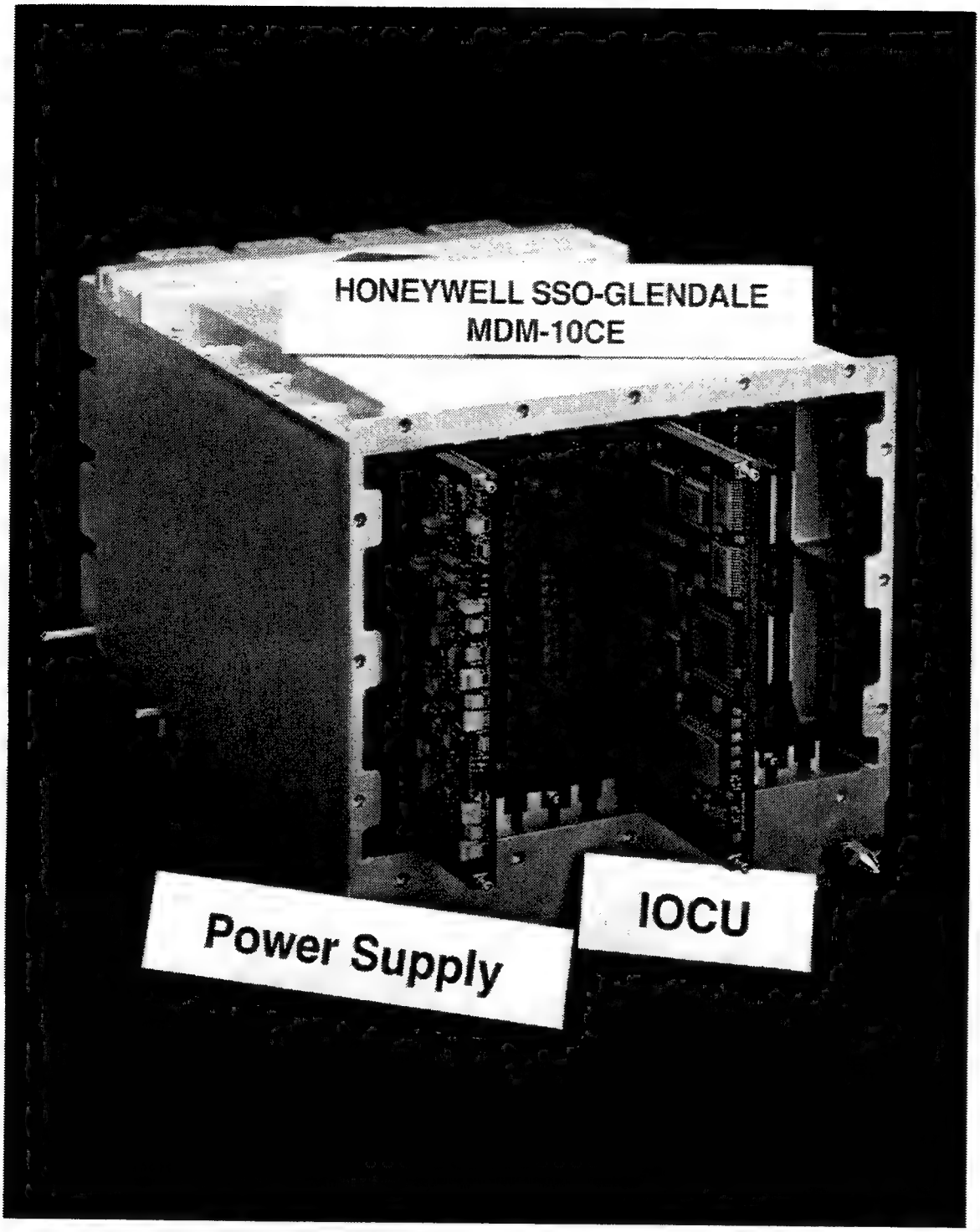
09-27245-8C/SC✚

FIGURE 1. Twenty Seven Layer Rigid Flex Motherboard



09-27245-7C/SC✚

FIGURE 2. ORU Connector



09-27245-1C/SC✤

FIGURE 3. MDM - IOCE 10 Slot Multiplexer/Demultiplexer

TABLE 1. Harness/ORU Assembly

Rigid-Flex Motherboard	PWB Layers	Flex Layers	Soldered pins	Dimensions	PWB Thickness	ORU Height	Weight
4CE	27	15	1504	5.3 in. x 13 in.	0.170 in.	2 in.	3.0 lb
10CE	27	15	3178	5.3 in. x 13 in.	0.170 in.	2 in.	5.0 lb
16CE	27	15	4602	5.3 in. x 13 in.	0.170 in.	2 in.	7.5 lb

Each backplane rigid flex is comprised of 27 layers of signal, power, ground and shielding conductors. The Rigid Flex and ORU Connector (Figure 4) and Rigid Flex With Card Edge Connectors (Figure 5) are soldered to rigid sections that are connected with 15 integral flex layers. The ORU and card edge connectors contain 1504, 3178, or 4602 pins that are soldered to the rigid flex printed wiring board. Making that many solder joints, while continuing to meet quality requirements, is an accomplishment.

Process

Honeywell SSO uses a mass soldering process based on a conventional wave solder machine. The process consists of a fluxer, a pre-heat section, followed by a single wave solder pot. The CCA is conveyed through the machine via an adjustable pallet. The following process variables can be adjusted to provide acceptable solder joints:

- CONVEYOR SPEED
- SOLDER POT HEIGHT
- SOLDER WAVE PUMP SPEED
- PRE-HEATER TEMPERATURES
- SOLDER POT TEMPERATURE

Soldering Profiles.

Rate of temperature change, dwell times, and temperature levels are the three elements used to profile the ramp up, equalization, wave solder, and cool down phases of the soldering cycle. Our process parameters are set to achieve a top side board temperature between 77 °C to 107 °C before the assembly enters the solder wave. These limits are fixed by NASA's *Requirements for Soldered Electrical Connections Handbook*, NHB 5300.4. The conveyor speed, solder pot height, and solder pump speed are set to achieve a dwell in the solder wave of three to four seconds.

The following lists a brief description of the chemical, metallurgical, and thermal dynamics processes occurring during the solder cycle phases:

- **Ramp up**. The soldering cycle begins by raising the assembly temperature to 92 °C ± 15 °C, as measured by thermocouples on the topside of the assembly. The rate of temperature change is set for less than 2 °C per second. Within this temperature range and with the use of Infrared (IR) lamp heaters, we obtain a safe and rapid evaporation of flux volatiles. Due to the rapid heating during this initial period, thermal gradients within the assembly develop. By holding the temperature rise to 92 °C ± 15 °C, the unevenly distributed thermal energy accumulated to that point is given time to equalize, thus reducing the possibility of detrimental thermal shock to sensitive components as the assembly passes over the solder wave. During the dwell at 92 °C ± 15 °C, flux activators begin scrubbing and reducing oxides from the metal surfaces.

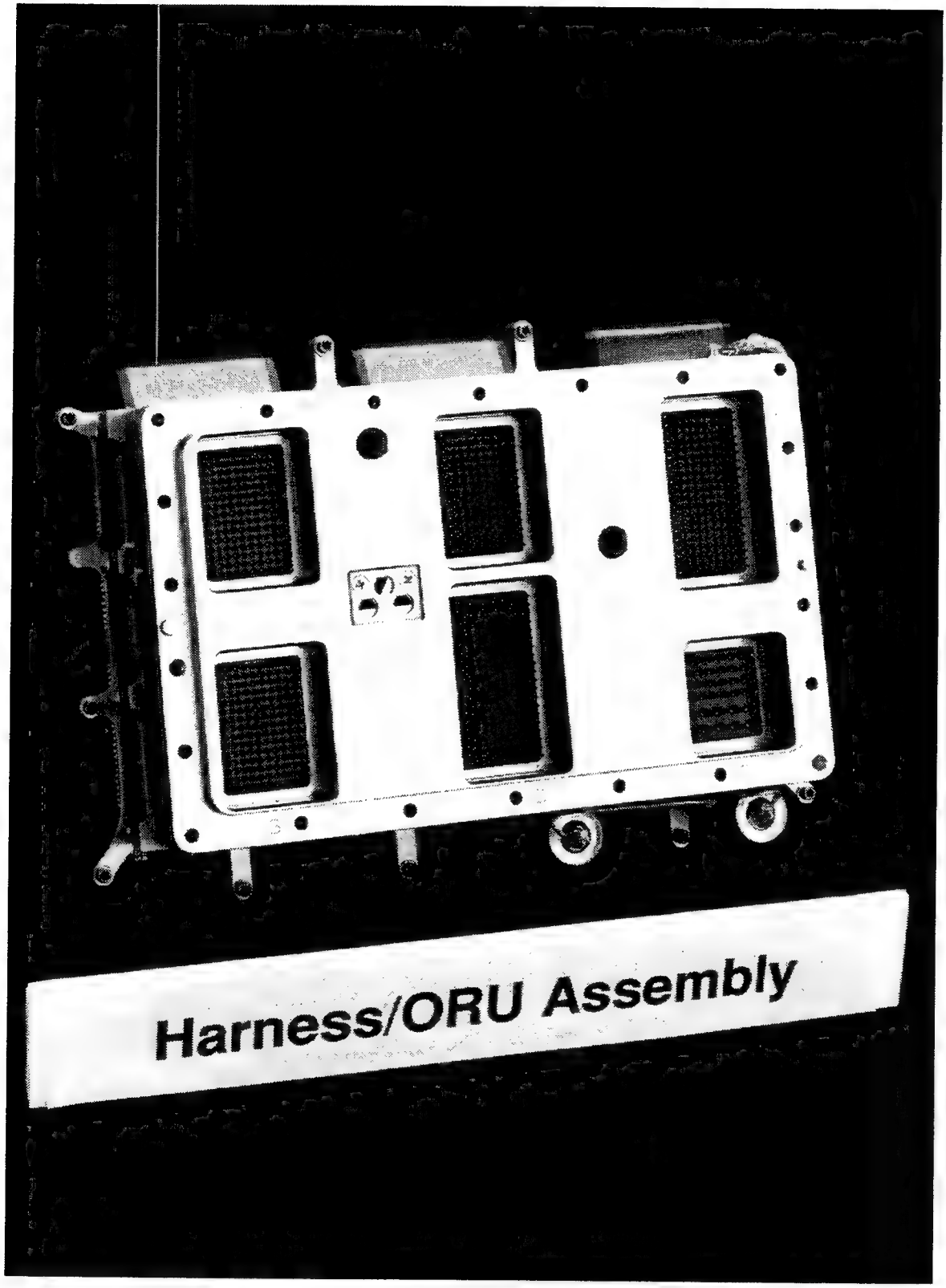
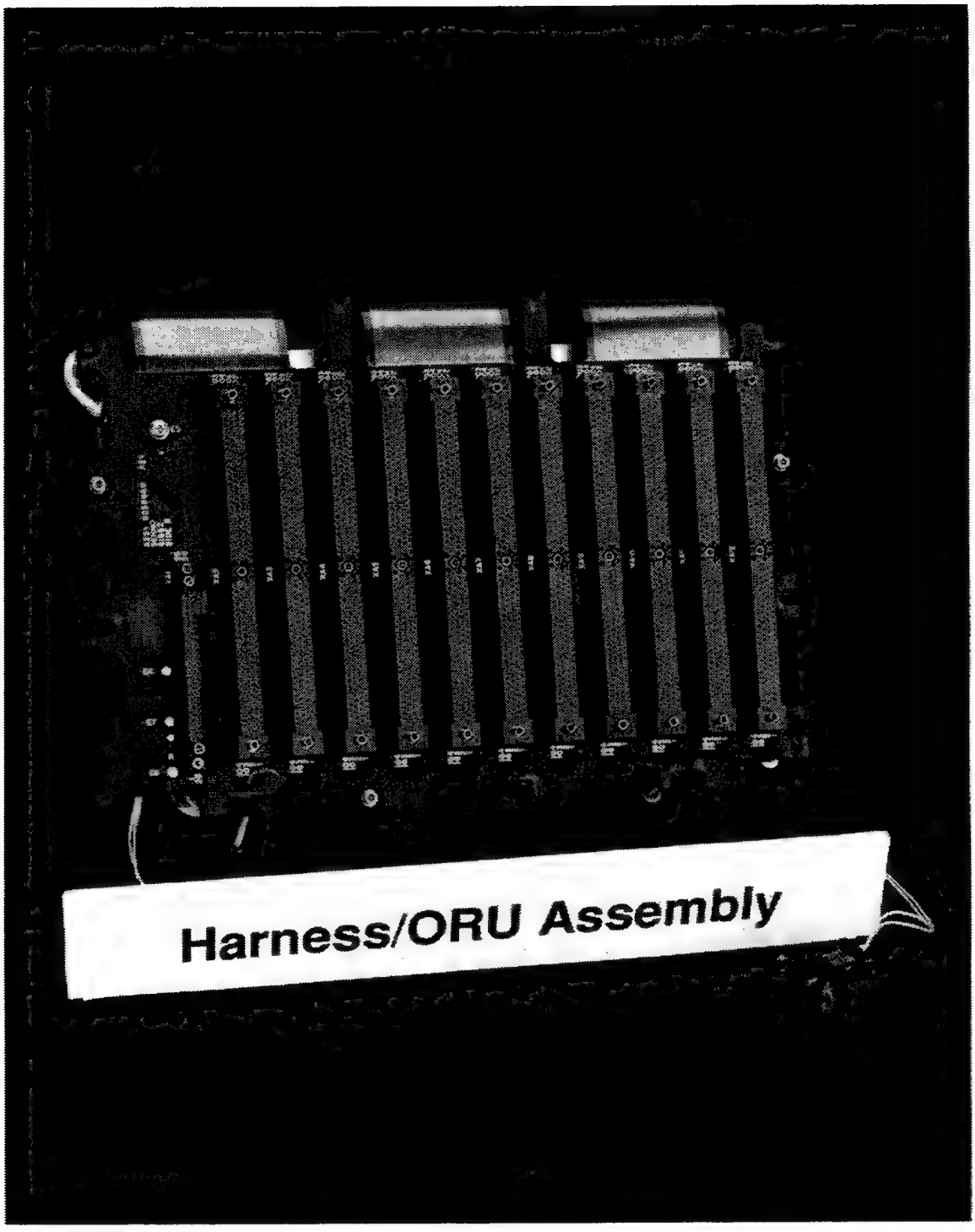


FIGURE 4. Rigid Flex and ORU Connector



09-27245-4C/SC✚

FIGURE 5. Rigid Flex With Card Edge Connectors

- **Equalization**. Assembly temperatures are now stabilized or are increasing at a much slower rate of 0.5 °C per second until the assembly crosses the solder wave. This time can be thought of as a thermal soak. It is during this period that materials with slower heat transfer characteristics can catch up with materials having faster characteristics so that the assembly does not experience delamination, or other types of thermally caused shock damage. Fluxes are fully activated, cleaning both termination pads and component leads. This entire soak period is accomplished in less than 30 seconds.

- **Solder Wave**. It is safe to rapidly raise the temperature of Printed Wiring Boards (PWBs) from 92 °C ± 15 °C to the solder wave temperature. In this relatively brief temperature rise, thermal differences within the PWB are not destructive. The measured PWB temperatures are usually much lower than 160 C° ± 15 °C; therefore, in the interest of minimizing both component exposure to elevated temperature and formation of copper tin intermetallics, the rate of thermal change is set at a rapid rate. Although the melting point of eutectic solder (Sn63, 63%tin 37%lead) occurs at 183 °C, most users operate with a solder temperature of 257 C° ± 6 °C to guarantee quick and total solder flow and the formation of acceptable solder joints. Typical solder flow occurs in less than six seconds at this temperature level. As the temperature reaches and ultimately surpasses the eutectic melting point, a molten mass of solder flows through the plated hole barrel, pushing flux away from the cleaned surfaces, wetting and covering them until all contiguous surfaces are covered with solder. The competing forces (i.e., surface tension, metallurgical-chemical attractions, capillary action component buoyancy, and gravity) have reached a state of equilibrium and the final solder joint configuration has been formed. It is at this moment that the cool-down period begins.

- **Cool down**. The initial phase of this last period involves a rapid cool down as the solder joint leaves the solder wave. It is just as critical to the quality and reliability of the solder joint as the earlier phases of the soldering cycle. The cool down rate should not exceed the rate of 3 °C per second. This cool down rate should be maintained until the solder joint reaches 160 °C; thereafter, the cool down is in accordance with a natural descent within the room environment.

Pre-heat Requirements

Before the solder flux becomes effective, chemical reactions take place within the flux to release acidic activators. With a mildly activated rosin flux, this requires a temperature above 88 °C. Preheaters provide the required thermal energy to activate the flux and drive off volatiles before the assembly crosses the solder wave. Honeywell SSO's wave solder machine has a 45 in. long preheat section made up of five flat ceramic panels of radiant IR heaters that heat the bottom of the assembly. Each heater contains a thermocouple providing a closed-loop feedback to the controller. The heaters radiate at a wavelength of 2 to 10 μm. Some top side heating is achieved by reflected IR and convective heating.

Flux Application

Solder fluxes must be applied to the underside of the board. The resultant flux coat must be uniform and thoroughly cover the areas to be joined. Honeywell SSO uses a foam fluxer to apply flux. A foam fluxer consists of a sump and a nozzle that contains a porous stone. The nozzle, or chimney, shapes and constrains the foam head. The fluxer is filled with an RMA flux until the porous stone is about two inches below the surface. Air is then pumped through the stone and a foam head rises out of the chimney to meet the underside of the PWB. The air pressure is adjusted to control the volume of air passing through the stone. A compressed air pressure of about 3 psig is sufficient to provide a uniform blanket of foamed flux. The bubbles of flux bursting within the plated through holes effectively coat the barrel and pin. An air knife lightly squeeggees flux from the assembly to ensure a uniform coating.

One of the controls of the foam fluxer is the maintenance of the specific gravity of the flux. At Honeywell SSO, flux specific gravity is monitored automatically. Flux must remain between 0.87 and 0.915. Because there is evaporation of flux volatiles, alcohol must be added periodically.

Solder Wave Parameters

The solder wave is generated in a large reservoir of molten solder. An air driven pump causes molten solder to flow up through a nozzle and baffles to provide a smooth wave 0.3 in. high. The printed wiring board assembly passes over the wave. It pumps solder up through the plated holes. The solder flows bi-directionally from the wave crest. The forward edge of the wave is turbulent forcing solder into the plated through holes. The trailing edge solder flow matches the board's conveyor speed so that excessive solder can be wicked from each lead.

TABLE 2. Wave Solder Parameters

Function	Standard PWB	ISSA Motherboard
Conveyor Speed	4 ft/minute	4 ft/minute
Flux Specific Gravity	0.870 to 0.915	0.89
Solder Pot Temperature	257 °C ± 6 °C	257 °C
Solder Wave Width	2.0 in. to 2.5 in.	4 in.
Preheater 1	260 °C to 338 °C	385 °C to 427 °C
Preheater 2	260 °C to 338 °C	385 °C to 427 °C
Preheater 3	260 °C to 338 °C	385 °C to 427 °C
Preheater 4	260 °C to 338 °C	385 °C to 427 °C
Preheater 5	260 °C to 338 °C	385 °C to 427 °C

Solder Joint Quality

NASA established solder joint acceptance in the *NASA Handbook 5300* for the ISSA. It differs little from other government and military specifications.

NASA Handbook 5300 (NHB 5300.4).

3A1005 INSPECTION CRITERIA

1. Acceptance Criteria.

   a. The appearance of the solder joint surface shall be smooth, non-porous, undisturbed and shall have a finish that may vary from satin to bright depending on the type of solder used.

   b. Solder shall wet all elements of the connection, except as noted in paragraph 3A1005-1f(2). The solder shall fillet between connection elements over the complete periphery of the connection.

f. PTH soldering

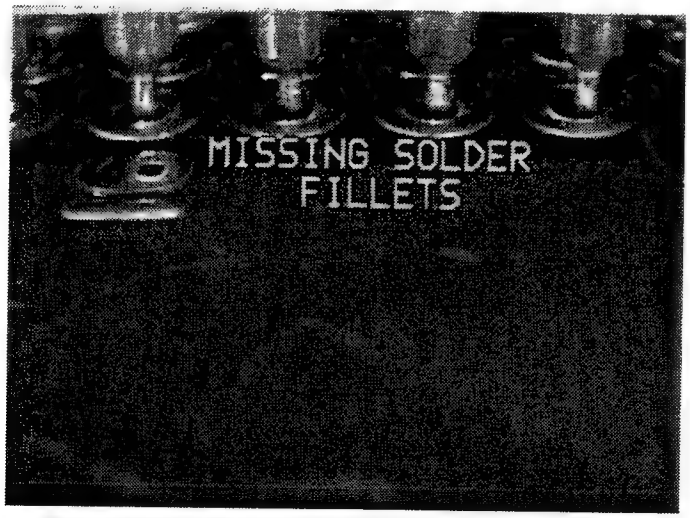
(1) On the solder application side, the quantity of solder shall meet all requirements established by this document.

(2) On the side opposite from the solder application, the solder shall, as a minimum, exhibit flow through and bonding of the lead or conductor to the solder pad. A slight recessing or shrink back of the solder into the PTH below the solder pad is acceptable, providing the solder obviously wetted the lead and onto the solder pad and the shrink back is slight enough that it can not be construed to be a solder void or blowhole. Also, slight dewetting of the solder around the periphery of the pad on the part side of periphery of the pad on the part side of the PWB is not cause of rejection.

This criteria is clear: bottom side solder joints should be perfect. Topside solder joints can be recessed, but if they are, acceptance depends on a subjective criteria. "Beauty is in the eye of the beholder." With several thousand soldered joints, it's best to have a full topside fillet. An incomplete fill could indicate a cracked plated through hole barrel and that would be a reliability issue.

The Problem

Using our normal wave soldering parameters, we were unable to obtain our targeted topside temperature of 107 °C before hitting the solder wave. The results were missing fillets and recessed topside solder joints, shown in Figure 6 and Figure 7, that were not acceptable for a manned space application. Topside temperatures were measured at the card edge connectors and under the ORU Connector. The profile showed the slower thermal response under the ORU Connector due to its large thermal mass. Even with an 85 °C preheat, the average temperature under the connector was less than our 77 °C to 107 °C target, as seen in Graph 1. The measured profile is not close to our typical profile.



S694-12-5/SC✤

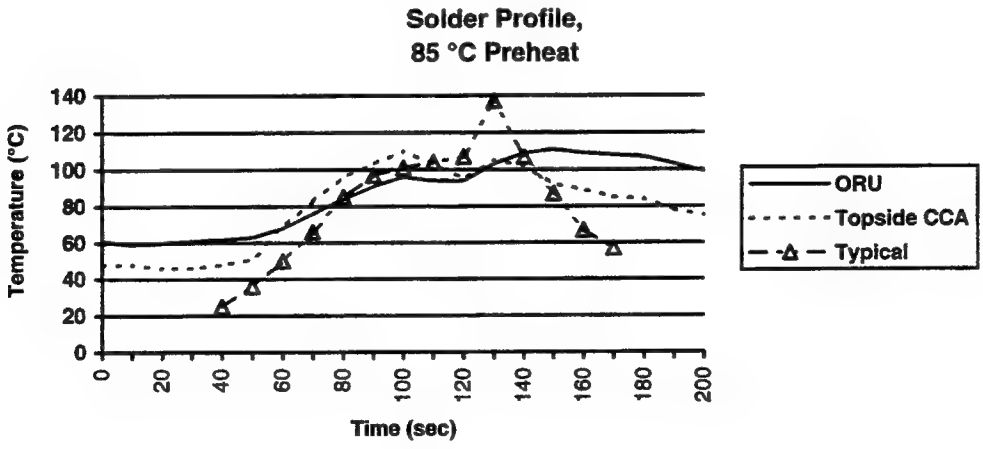
FIGURE 6. Missing Solder Fillets Under ORU Connector

S694-12-6/SC✚

FIGURE 7. Recessed Solder Fillets Under ORU Connector

Our five preheaters were at their maximum temperature of 427 °C. Our standard conveyor speed of four ft/min was already slower than industry norms. The solder pot temperature of 257 °C could be raised closer to the maximum of 263 °C allowed by *NASA Handbook 5300 (NHB 5300.4)*. That would increase dross formation and would place us outside our window of experience. The dwell in the solder wave could be extended from 2 to 3 seconds to as much as 5 to 6 seconds.

GRAPH 1. Wave Solder Profile with an 85 °C Preheat

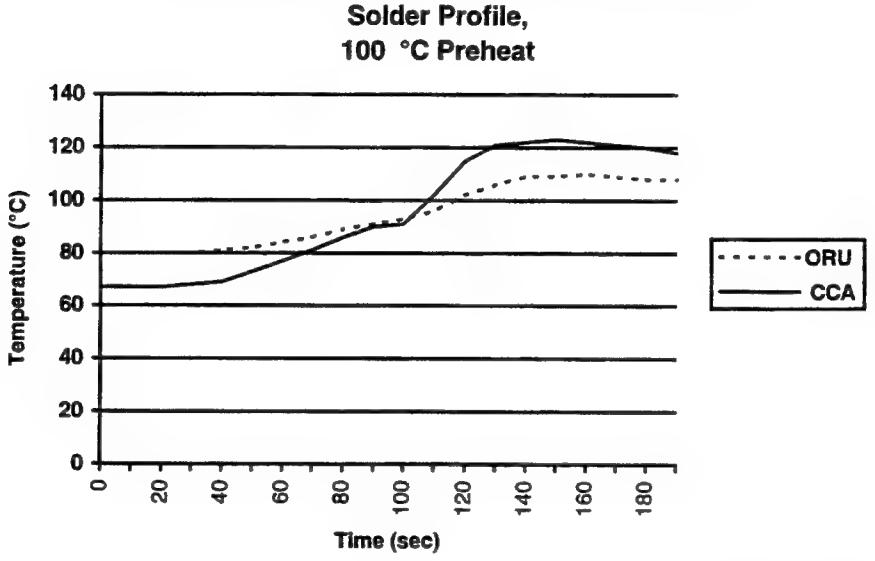


S694-12-7/SC✚

The Solution - Oven Preheat

Our basic problem was that the thermal mass of the assembly exceeded our equipment's thermal capability. We extended that capability with an oven preheat. By placing the entire assembly in an 95 °C ± 5 °C oven, we can provide the 100 °C topside temperature required to achieve a plated through hole completely filled with solder. At the same time, the oven heating provides a uniform assembly temperature to reduce thermal expansion mechanical stresses. The resulting profile in Graph 2 demonstrates the efficacy of this simple solution.

GRAPH 2. Wave Solder Profile with an 100 °C Preheat



Foam Fluxer

Although the oven preheat provided a good solder thermal profile, it caused new problems. Not only did we now have a hot assembly to load into the wave solder conveyor, the foam head in our fluxer collapses if an assembly is above room temperature. We were not prepared to run without flux. Our fix was to first run the assembly over the foam fluxer at room temperature. Then, place the fluxed assembly in a nitrogen backfilled oven. Using nitrogen backfill prevents oxidation of the lead and PWB solder as flux becomes more active at the 100 °C oven temperature.

CONCLUSION

The flux application followed by an inert oven preheat provided acceptable plated through hole solder fill. Inspection of topside solder joints at the connector perimeter showed good wetting and fill. Normal optical inspection cannot determine the acceptability of joints in the middle of the connectors. We have used 0.093 in. and 0.040 in. optical fiber probes to inspect sample joints. This is not the process for 100% of inspections. We plan to use X-ray laminography or X-ray microscopy to inspect and accept production assemblies.

Chris Alter is a Principal Manufacturing Engineer for Honeywell, Inc.

A member of IEEE, ISHM, and the Phoenix Chapter of ISHM, he is technical chairman of SME. He is the recipient of the Armed Forces Electronics Association Honor Award.

He has a bachelor of science degree in mechanical engineering from the University of Michigan and a master's degree in business administration from the University of California, Berkeley.

Address: Honeywell, Inc.
Satellite Systems Operation
P.O. Box 52199
Phoenix, AZ 85072

Joe Naperkowski is a Lead Manufacturing Engineer for the ISSA MDM program and a Principal Manufacturing Engineer for Honeywell, Inc., with 4 years' experience as a quality control analyst; 4 years' experience as a quality engineer-developer, implementing quality systems and programs, and introducing new production; 2 years' experience in project management; and 15 years' experience in manufacturing process, and product development and support.

He has a bachelor of science degree in electrical engineering from Bridgeport Engineering Institute, Bridgeport, Connecticut.

Address: Honeywell, Inc.
Satellite Systems Operation
P.O. Box 52199
Phoenix, AZ 85072

INSPECTION CAPABILITY

by

Russell D. Brady
Quality Assurance Manager
Scanivalve Corporation
San Diego, California

ABSTRACT

Considerable attention is given to all forms of soldering processes and inspection systems, both manual/visual and automated. In-circuit and stress testing are important tools for detecting unreliable assemblies through the discovery of inferior solder connections or components. Unfortunately, these methods do not discriminate between levels of performance to workmanship standards such as MIL-STD-2000 or 2000A. For that we must rely upon the human eye and rationale of in-process inspectors.

We tend to judge an inspector's ability on such criteria as the number of defects found during inspection and we think of quantity as quality. It is more often true that "tough" inspectors reject marginally acceptable conditions causing un-necessary rework, while "easy" inspectors pass marginally unacceptable conditions which may require attention later in the process or at the customers' site.

There is a method for determining the capability and biases of inspectors with considerable accuracy. It will characterize an inspector's ability to discern faults and reveal individual biases toward leniency and stringency. A typical result of performing such a study, is the revelation that the seemingly average inspector is often found to do the better overall job while the "tough" or "easy" inspectors are found lacking.

WHY ANOTHER STUDY?

This particular study assesses the individual and collective capability of the inspection department. It will point to training opportunities as well as provide valuable insight into matching personalities to specific inspection assignments. For the sake of efficiency alone, a study of this nature is an absolute necessity. If the invisible factory (rework) is a large part of your operation, inspection is often a factor, directly or indirectly. In direct causes, one speaks to training, perception, and biases. Indirectly we find factors such as; the absence of inspection criteria, ambiguous criteria, and the lack of adequate inspection aids. Ultimately, a study such as this provides a thorough review of the inspection process as well as the documentation which provides criteria for the inspection.

PREPARING FOR THE STUDY

For the purpose of this discussion, we will focus upon the printed circuit board assembly. Select an assembly or a portion of an assembly having moderate component density and a component count less than 100 items.

Using the best qualified people, other than the inspectors, such as engineers, soldering instructors, etcetera, study the documentation for the assembly, workmanship standards, and/or MIL-STD-2000 and form agreement upon the definition of conformance for each type of placement and soldering.

Select 12 to 24 assemblies and attach removable number tags to the assemblies. Remove or cover any markings which would serve to distinguish on assembly from another. If a marking is found on one assembly only, apply a covering to the marking on that assembly and all other assemblies involved in the study.

Using the established criteria, perform a thorough inspection of the target area. Each member of the evaluation team must inspect each assembly and results must be compared. Any differences in evaluators perceptions and findings must be resolved. Defects found during the screening should be left as they are unless the numbers of defects exceed the study requirement. Of the assemblies selected, one-third should have one defect, one-third should have no defects, and the remaining one-third should have one marginally good or marginally bad condition. The latter will be determined by your criteria and will require that a very good solderer pushes the envelope just short of and beyond the break point. (Hopefully some of these will be found in the assemblies selected for the study.) It is beneficial to have a somewhat equal distribution, but not essential. The evaluation team must, once more, inspect the assemblies and reach agreement on the final conditions.

Prepare data collection sheets which allow for the inspector's identity, and inspection pass number. There must be a block for each assembly which the inspector will fill with "R" for reject, and "A" for accept.

CONDUCTING THE STUDY

- Assemble the inspectors who are to be involved in the study.
- Define the purpose of the study.
- Supply the inspectors with all relevant reference material and criteria for the assembly. For assemblies on which a selected portion only is to be observed, mask the area not to be observed or provide a template.
- Assign start times for each inspector. (not all can work simultaneously)
- Present the assemblies a number 1 through (n) for the first pass. *DO NOT REVEAL THE NUMERICAL DISTRIBUTION OF DEFECTS.*

- Allow each inspector to inspect each assembly and record the findings.
- Collect the data collection sheets from each inspector upon completion. Be sure the sheets identify the inspector and pass number. *DO NOT ALLOW THE INSPECTORS TO DISCUSS THE STUDY OR COMPARE NOTES UNTIL THE STUDY IS COMPLETED AND VERIFIED.*
- When all inspectors have finished the first pass and all sheets have been collected, change the assembly number tags. Be very careful to properly record the original number of the assembly and the number to which it has been changed. If you lose track at this point you will have to restart, perhaps at the beginning.
- After the second pass, repeat the foregoing once more changing the numbers.
- After the third pass, you may release the inspectors and retire to consider the data.

CRUNCHING THE DATA

Prepare the tally sheet, entering the assembly number in the first column and the actual rejection/acceptance finding in the second. Enter the result of the first pass for each inspector in the original order of the assemblies followed by the second and third passes. Be sure to convert the numbers from the second and third passes back to the original number, otherwise the result will not make sense. Having completed this task, we turn our attention to the calculation sheet.

For each appraiser, enter the false alarm (FA) and MISS opportunity totals. For example, if eighteen assemblies are used for the study, and half of those have a combination of hard defects and marginally bad conditions, there are nine opportunities for FA and nine opportunities for MISS. Since there are three passes, multiply the numbers of opportunities by three, thereby providing twenty-seven opportunities each.

From the tally sheet, count and record the total number of rejections of acceptable assemblies for all three passes for each inspector under FA. Count and record the number of acceptances of rejectable assemblies under MISS. For each inspector, divide the actual FA by the opportunity FA, round the result to two decimal places and enter the result in FA under probability. Divide the actual MISS by the opportunity MISS and enter the rounded result in MISS under probability.

Interpretation of results from this point is fairly simple. 0.02 or less for FA is acceptable. 0.01 or less for MISS is acceptable. 0.05 or less and 0.03 or less, respectively are marginal, leaving anything higher, unacceptable. It can be reliably inferred that a significant imbalance between the FA and MISS probabilities is indicative of a bias toward criticality or leniency.

It is best to withhold any formal report at this time as there is yet one vital function to perform.

FOLLOW-UP

Gather the inspectors for an open discussion of the study. At this time, reveal the details of the defects and distribution and the findings. Be prepared for some discussion and the need to produce the assemblies for some show and tell. You will surely be required to explain your rationale particularly as regards marginal conditions. Also, as may happen, most of the participants in the study will have found a defect which escaped the notice of the team or want to dispute a listed defect. Take the time to discuss and understand the issue. If the participants challenge is supported, and the team agrees, change the data collection sheets and findings accordingly. Make necessary notes in the records to explain the action.

WE'VE DONE THE STUDY, WHAT NOW?

If the results are unsatisfactory for all of the participants. a total review of criteria should be undertaken and, if indicated, conduct training for all of the participants. If one or two fail, a directed training effort should remedy the situation. For those who demonstrate biases, training may help but, there may not be a real solution. Very often the bias is a personality trait which is not easily overcome. The affect of the corrective action will not be totally measurable until the study is repeated. When necessary, the study should be repeated about six months after the first study. Do not repeat the study until training has been completed and necessary document changes have been implemented. A study such as this is very expensive and highly disruptive and as such should be used to the greatest effect. In short, learn all you can each time the study is conducted.

SUMMARY

In this short period of time, we have had a look at an evaluation method which can add significantly to inspection efficiency. It is necessary that we understand and evaluate every facet of the manufacturing process. This particular study is not by any means limited to printed circuit board assemblies as suggested in this treatment. It can be applied to virtually any process or product which yields attributes data. Regardless of the target and purpose of the study, the requirement is the same: plan the study, research the requirement and criteria, prepare the material, execute the study, follow-up and adjust, report the findings, and, always, take corrective action.

INSPECTION SHEETS
(cut-out)

INSPECTOR NUMBER 1

SAMPLE NUMBER AND FINDING
A=ACCEPT, R=REJECT

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	17	18	19	20

INSPECTOR NUMBER 2

SAMPLE NUMBER AND FINDING
A=ACCEPT, R=REJECT

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	17	18	19	20

INSPECTOR NUMBER 3

SAMPLE NUMBER AND FINDING
A=ACCEPT, R=REJECT

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	17	18	19	20

INSPECTOR NUMBER 4

SAMPLE NUMBER AND FINDING
A=ACCEPT, R=REJECT

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	17	18	19	20

INSPECTOR NUMBER 5

SAMPLE NUMBER AND FINDING
A=ACCEPT, R=REJECT

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	17	18	19	20

TALLY SHEET

20 SAMPLES, 3 TRIALS

NO.	A/R	INSPECTOR 1			INSPECTOR 2			INSPECTOR 3			INSPECTOR 4			INSPECTOR 5		
1																
2																
3																
4																
5																
6																
7																
8																
9																
10																
11																
12																
13																
14																
15																
16																
17																
18																
19																
20																

INSPECTION CAPABILITY CALCULATION SHEET - ATTRIBUTE DATA

OPERATION: _____ DATE: _____

DATA CALCULATIONS

APPRAISER	OPPORTUNITIES		ACTUAL		PROBABILITY	
	FA	MISS	FA	MISS	FA	MISS
TOTAL						

The criteria for acceptability of an inspection capability study with attribute data is as follows:

P (FA)	P (MISS)	STUDY RESULT
0.02 or less	0.01 or less	Acceptable
Between 0.02 and 0.05	Between 0.01 and 0.03	Marginal
Greater than 0.05	Greater than 0.03	Unacceptable

Russell D. Brady is a Quality Assurance Manager for Scanivalve Corporation, San Diego, California. He has 5 years' experience as a senior manufacturing engineer, 4 years' experience as a senior quality engineer, and 4 years' experience as a quality assurance manager. He is an ASQC-certified quality engineer soldering technology, Category C, and an ISO-9001-certified assessor.

He attended Chaffey College, Riverside Community College, and Cal Poly, Pomona, Calif.

Address: Scanivalve Corporation
10222 San Diego Mission Road
San Diego, CA 92108

APPLICATIONS OF PRACTICAL STATISTICS

Tom Clifford
Process Specialist
Lockheed Missiles and Space
Sunnyvale, Ca.

Abstract

This paper discusses two applications of shop-floor statistics. In the first, we demonstrated in a comparative study how DOE can be a powerful cost-saver: a D-Optimal design with 18 samples gave exactly the same results as did a full-factorial matrix requiring 48 samples. In the second, we report a new method for estimating the accuracy of very low-defect-ppm values. Specifically, using simple spread-sheet software or the graphs provided, one can determine the confidence bounds around very low ppm values as a function of run length (sample size).

DESIGN OF EXPERIMENTS

Several years ago, we began to hear about Design-Of-Experiments, as a tool for process experimentation. We were told that using the proper mathematical planning, sample selections and conditions, we would see substantial cost-savings because fewer experimental samples would be required. However, full utilization of DOE has been difficult, primarily because of the perception that the mathematics and software are forbidding. Furthermore, old-timers tend to distrust it. Most of us have been raised on 1-FAT principles (vary one factor at a time). It is not intuitively clear that one can obtain good information from so few samples, particularly varying many parameters at once.

During some early process development work, we had an opportunity to prove the value of DOE. To characterize a thermal rework process, we needed to understand the effect of and interactions among four factors at several levels each. We initially planned a 48 sample full-factorial matrix (two nozzles sizes, four gas flow-rates, three power settings, two impingement locations). Our process statistician, using commercially-available software, following the proper rules and prompts, selected a D-optimal plan that said only 18 of the 48 samples would be needed. Figure 1 shows the full matrix as well as the 18 points selected by the software. We saw this a neat test case: this particular experiment was not that expensive to run as a complete matrix; we could compare the two approaches. Therefore, data was obtained on all 48 points. Using the software, we analyzed the data from only the selected 18 samples, in order to see whether the "missing" data could be predicted by the DOE software. Figure 2 shows the actual measured test data, as well as data predicted by a best-fit analysis from the 18 selected samples. the D-Optimal plan predicted the missing 30 data points within a couple of degrees. Further, to help visualize the process interactions, we used the software capability to generate response surfaces. Figure 3 shows that response surfaces derived from the 18 DOE-selected points were indistinguishable from those derived from all 48 data points.

This exercise has demonstrated that a little technical finesse can give the same results as would a brute-force approach. This exercise has helped the conversion of our technical staff to an appreciation of the value of DOE in process development.

THERMAL STUDIES - DOE SELECTION MATRIX											
#	NOZZLE	LOCATION	HEAT SETTING	FLOW	D-OPT	#	NOZZLE	LOCATION	HEAT SETTING	FLOW	D-OPT
1	BIG	CENT.	6	20	<<	25	LITTLE	CENT.	6	20	<<
2	BIG	CENT.	6	12		26	LITTLE	CENT.	6	12	
3	BIG	CENT.	6	6		27	LITTLE	CENT.	6	6	
4	BIG	CENT.	6	3	<<	28	LITTLE	CENT.	6	3	<<
5	BIG	CENT.	8	20		29	LITTLE	CENT.	8	20	
6	BIG	CENT.	8	12		30	LITTLE	CENT.	8	12	
7	BIG	CENT.	8	6		31	LITTLE	CENT.	8	6	
8	BIG	CENT.	8	3		32	LITTLE	CENT.	8	3	<<
9	BIG	CENT.	10	20	<<	33	LITTLE	CENT.	10	20	
10	BIG	CENT.	10	12		34	LITTLE	CENT.	10	12	<<
11	BIG	CENT.	10	6		35	LITTLE	CENT.	10	6	
12	BIG	CENT.	10	3	<<	36	LITTLE	CENT.	10	3	
13	BIG	TWEEN	6	20	<<	37	LITTLE	TWEEN	6	20	
14	BIG	TWEEN	6	12		38	LITTLE	TWEEN	6	12	<<
15	BIG	TWEEN	6	6		39	LITTLE	TWEEN	6	6	
16	BIG	TWEEN	6	3	<<	40	LITTLE	TWEEN	6	3	<<
17	BIG	TWEEN	8	20		41	LITTLE	TWEEN	8	20	<<
18	BIG	TWEEN	8	12	<<	42	LITTLE	TWEEN	8	12	
19	BIG	TWEEN	8	6		43	LITTLE	TWEEN	8	6	
20	BIG	TWEEN	8	3		44	LITTLE	TWEEN	8	3	
21	BIG	TWEEN	10	20	<<	45	LITTLE	TWEEN	10	20	<<
22	BIG	TWEEN	10	12		46	LITTLE	TWEEN	10	12	
23	BIG	TWEEN	10	6		47	LITTLE	TWEEN	10	6	
24	BIG	TWEEN	10	3	<<	48	LITTLE	TWEEN	10	3	<<

FIGURE 1. Test matrix, showing the full-factorial 48-sample plan, as well as the 18 samples selected in the D-optimal DOE plan.

THERMAL STUDIES - TEMPERATURE COMPARISONS							
#	ACTUAL TEMP.	D-OPTIMAL PREDICTION	DELTA	#	ACTUAL TEMP.	D-OPTIMAL PREDICTION	DELTA
1	157	156	-1	25	163	165	2
2	154	154	0	26	154	159	5
3	144	143	-1	27	143	144	1
4	137	133	-4	28	132	133	1
5	223	226	3	29	249	245	-4
6	214	207	-7	30	220	222	2
7	187	183	-4	31	197	195	-2
8	163	168	5	32	173	173	0
9	282	285	3	33	316	314	-2
10	250	250	0	34	276	275	-1
11	213	213	0	35	237	235	-2
12	195	192	-3	36	206	210	4
13	152	149	-3	37	154	152	-2
14	149	151	2	38	147	149	2
15	139	142	3	39	139	137	-2
16	135	134	-1	40	130	127	-3
17	209	211	2	41	226	224	-2
18	200	196	-4	42	198	205	7
19	172	175	3	43	184	180	-4
20	153	158	5	44	170	165	-5
21	262	262	0	45	284	286	2
22	230	231	1	46	250	250	0
23	200	197	-3	47	217	213	-4
24	180	177	-3	48	189	191	2

FIGURE 2. Comparison between the actual measured values, and the predicted values, obtained from the 18-sample D-optimal plan

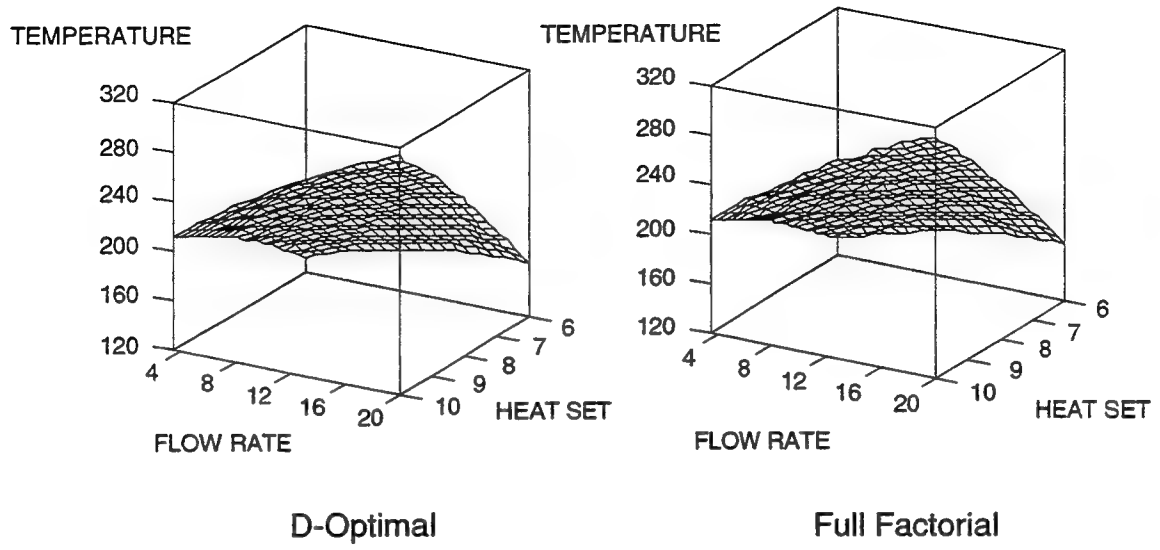


FIGURE 3. response surfaces derived from all 48 data-points and from only the 18 datapoints

DEFECT STATISTICS

The quest for 6-sigma performance has focused attention on reporting and comparing low ppm values. Examples of the need to understand what these ppm values really mean are all around us. Often we compare suppliers or processes based on reported defect ppm values. Leaving aside all technical questions, we want to know how statistically meaningful those ppm values really are. We report "0 ppm" on a production run with zero defects. Can we really say that we are 95% confident that this process really is running 0 ppm? Start-ups typically involve qualification runs. We want to know how many assemblies to make and inspect in order to "get enough data" to be confident that we've characterized the process. The math is simple: divide the number of defects by the number of opportunities and multiply by 1 million. The temptation is to report, and believe, and to compare that number. This simple approach is not statistically justifiable. Intuitively, one knows that larger sample sizes improve the confidence of the estimate, and that more data means more confidence (tighter confidence bounds or greater confidence levels) in your results. You are much more confident in the value of a calculated 0 or 100 ppm from a 500,000 pc run than you are in 0 or 100 ppm from a 2000 pc run. We wanted a convenient way to link sample size to confidence intervals, in defect statistics.

We found nothing in the electronics or popular statistics literature to establish confidence bounds around these sorts of numbers. Our statisticians came up with such a tool, applying cumulative binomial distribution mathematics. We now have software which is available in a plug-in spread-sheet format to do the necessary calculations. Given a sample size and a number of defects, the program calculates the ppm value, and more importantly the upper and lower bounds of the ppm value at several confidence levels.

As one example: zero defects in a run of only 10,000 pcs must be understood as actually anywhere from 0 ppm up to 350 ppm, if you want to be 95% confident. If there are still zero defects after 100,000 pcs, the estimate is much more persuasive: the process can be said, with 95% confidence, to be running from 0 to 50 ppm. Extending that, if there are zero defects after a run of 2,000,000 pcs, you can say with 95% confidence that the process has shown it is running at between zero and approx 5 ppm. This trend of tightening confidence with increasing sample size is shown in Figure 4. This figure, which was generated from the soft-ware, also dramatizes the importance of confidence intervals. Considering our example of zero defects in a run of 10,000 pcs: with 95% confidence, we can say the process is at 0 to 350 ppm. However, if you demand 99% confidence in your statement, you must say only that the process has shown it is between 0 and 530 ppm. On the other hand, if you don't mind being wrong half the time, you can say with 50% confidence that the process is between 0 and130 ppm. The graph provides an understandable method for visualizing these interactions.

The software allows analyses of any set of cases, depending on your inputs, selected to fit your particular question. Figure 5 describes some cases built arbitrarily around 1000 ppm. If 1000 ppm is calculated on a short run of 5000 pcs, the graph shows that the defect level is somewhere between 250 and 2300 ppm, to be 95% confident. If you calculated 1000 ppm from a run of 100,000 pcs, the 95% confidence limits tighten to 850 to 1200 ppm. In general, the more data points, the better your knowlege of your system.

This new data treatment is a useful tool in planning and interpreting defect rate data. It allows rational comparison of defect rates taken from different sized populations. It tells you how confident you can feel given a particular defect rate result. It can tell you how many samples you must run in order to be able to make a statement on a particular defect rate, with the usual (95%) confidence. The software is available on request.

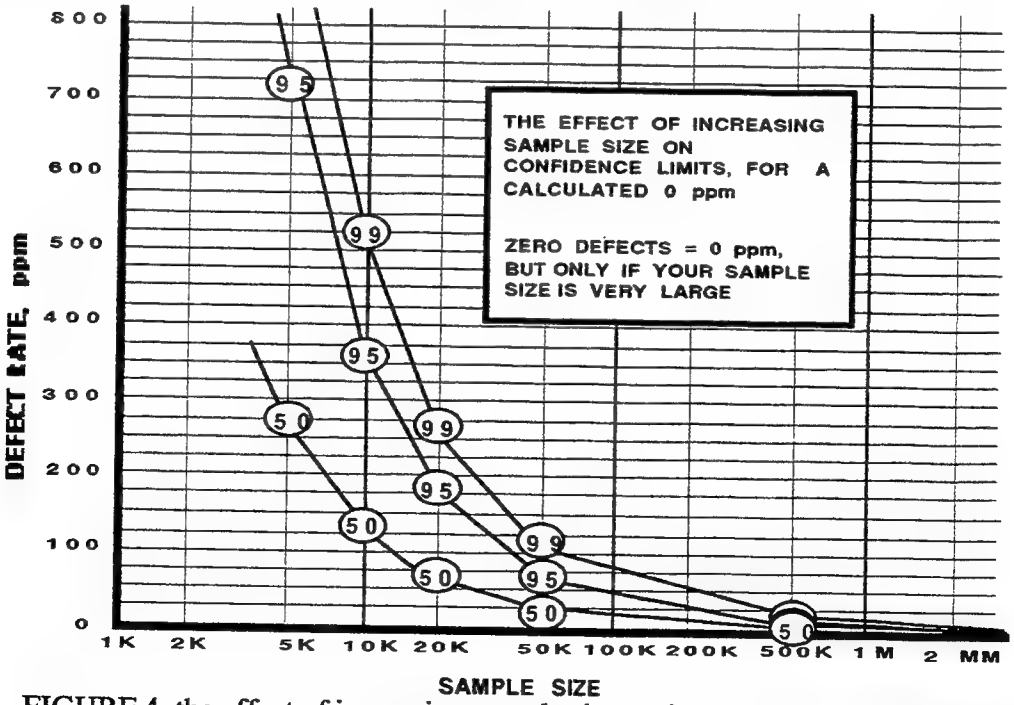


FIGURE 4. the effect of increasing sample size on improvement in confidence in 0 ppm defect levels.

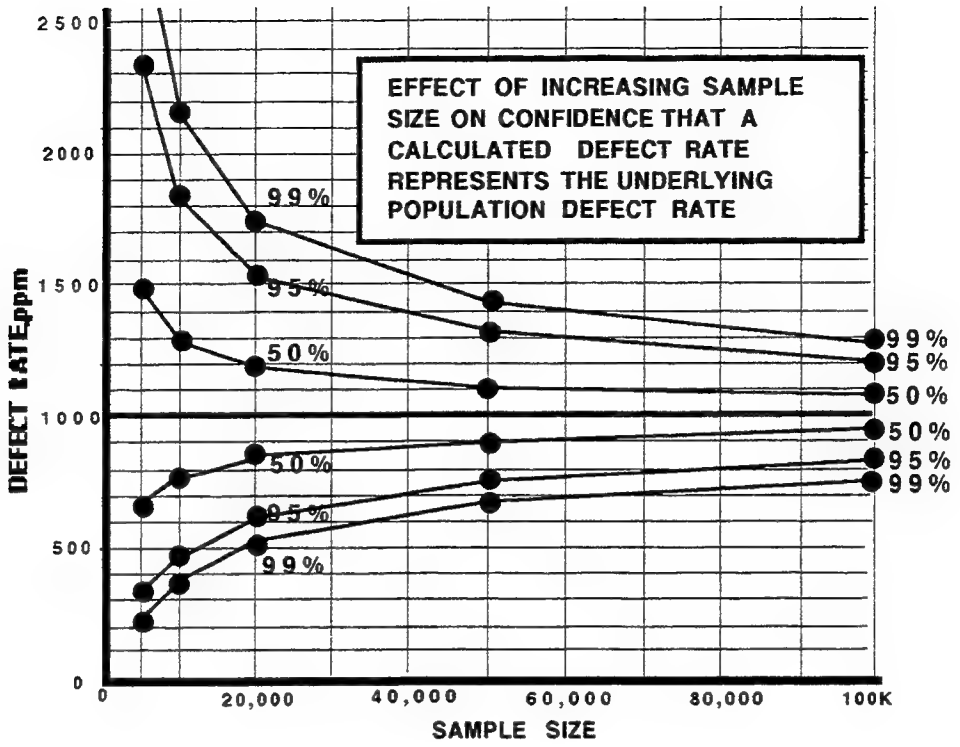


FIGURE 5. The effect of increasing sample size on improvement in confidence, at 1000 ppm defect levels.

Tom Clifford is a Process Specialist for Lockheed Missiles and Space Company. He has 15 years' experience in plastics product and process development and 15 years' experience in electronics product development and manufacturing. He has several patents for plastics processing and a patent for a board interconnect device.

He has a bachelor of chemical science degree from Texas Tech, Lubbock, Texas.

Address: Lockheed Missiles and Space Company
1111 Lockheed Way
Sunnyvale, CA 94286

-Technology Update -
Parylene Conformal Coating for Chemical Agent Protection

by Roger Olson, Director of Technology and New Business
Specialty Coating Systems, Inc.
Subsidiary of Alpha Metals, Inc.
Indianapolis, IN

ABSTRACT

Protection of "Mission Essential" assemblies from the adverse effects of corrosive chemical warfare agents and related decontamination solutions requires high performance protective coatings, particularly since such coatings must not interfere with the performance of protected materials and surfaces.

This paper reviews the requirements of NAV. INST. 3400.2, USAF-80-30, Army Reg. 70-71 and MIL-I-46058C. It discusses use of vacuum deposited poly-para-xylylene (Parylene) conformal coating to satisfy the requirements of these specifications for chemical agent protection of electronic circuits and related surfaces. The non-solvent, non-ODC Parylene coating process is explained, along with performance characteristics of the deposited protective film. Pertinent chemical warfare agent test procedures and results are also described.

BACKGROUND

The protection of mission-essential materials from the adverse effects of chemical warfare agents and their decontamination solutions is a challenging aspect of electronic manufacturing. Possession of sophisticated offensive weaponry is of no value if it cannot be deployed because critical systems have been compromised by the corrosive effects of these agents.

The approaches to chemical agent protection are many and varied. One of the most used approaches is to simply construct material from substances that are inert or resistant to chemical agents. Materials that are inert are unaffected even after prolonged exposure to chemical agents. Resistant materials will survive for some period of time, but not indefinitely.

If, for various reasons, critical material cannot be fabricated of inert or resistant materials, another approach is to encase them in a chemically hardened enclosure, sometimes with elaborate filtration systems. This approach can lead to problems should field service become necessary in a contaminated area. It also adds weight and cost to protected components.

A third approach is the use of various protective coatings, which is the means by which SCS/NOVA TRAN™ Parylene Coating Services became aware of the chemical agent protection program. SCS was approached by a contractor producing a new generation military gas mask. A component of the mask called a "voicemitter" (Figure 1) contained a mylar diaphragm that is susceptible to attack by chemical agents.

The diaphragm allows voice communication between individuals wearing the heavy protective mask, which would otherwise distort the human voice and make communication very difficult.

Chemical agents would attack the diaphragm causing it to craze and fail. The diaphragm had to be protectively coated over its entire surface while enclosed in a perforated metal housing.

This constraint prohibited use of conventional liquid or spray coatings because it would be impossible to ensure 100% coverage inside the aluminum housing. In addition, these liquid coatings interfere with the function of the unit due to the inability to control and minimize thickness across the diaphragm's radius. It was determined that a thin coat (2.5 microns) of parylene would render the mylar inert to various chemical agents while ensuring that each diaphragm was 100% coated, with no effect on mechanical functionality.

PARYLENE VACUUM DEPOSITED FILM

Parylene is the generic name for the various members of a polymer series (para-xylylenes). Parylene has been in commercial use for about 25 years. Primary application for this polymer has been in the military, aerospace, medical, electronics and automotive industries to protect various substrates and devices from all forms of hostile environments.

POLYMER PHASE CHARACTERISTICS

The precursor (dimer) phase of parylene, di-para-xylylene is a white powder. When converted to the polymer form (poly-para-xylylene) the material exhibits very little absorption in the visible range and is therefore colorless and transparent.

The polymer form is extremely resistant to chemical attack and is insoluble in most known chemicals. Parylene exhibits a polycrystalline structure with a contact angle of 87°, and is extremely resistant to moisture in any form.

The material remains stable at continuous temperatures as high as 130 °C in air or 220°C in the absence of oxygen. Polymerization of the film is accomplished at room temperature and is solvent-free. As a result, no thermal, mechanical or chemical stress is placed on the substrate.

The monomer phase of parylene is an extremely active molecule that results in superior penetration power (ability to reach into deep surface recesses) and a high degree of conformability.

Parylene exhibits impressive mechanical strength and flexibility in a thin film coating. Tensile strength is 6.9 X $10^7 n/m^2$, and yield strength is 5.2 x $10^7 n/m^2$. The film elongation to break value is 200%, for a yield elongation of 2.9%.

The parylene polymers are deposited from the vapor phase by a process that resembles vacuum metalization in some respects (Figure 2). The parylenes are formed at a pressure of approximately 0.1 torr. Under these conditions the mean free path of gas molecules in the deposition chamber is on the order of 0.1 cm. Parylene is not line-of-sight. All sides of an item to be encapsulated are impinged by the active gaseous monomer, resulting in truly conformal coating. Coating thickness is within 10% on flat surfaces, radii, edges, sharp points and in slots and crevices.

The vacuum deposition process consists of three distinct steps, with the precursor material converted from solid to gas with no intermediate liquid phase. The first is vaporization of the powdered dimer at approximately 160°C .

The second is quantitative cleavage (pyrolysis) of the dimer at the two methylene-methylene bonds at about 680°C, to yield the monomeric diradical, para-xylylene.

Finally, the monomer enters the room-temperature deposition chamber where it simultaneously absorbs and polymerizes on the substrate. The substrate temperature never rises more than a few degrees above ambient.

MILITARY SPECIFICATION MIL-I-46058C

An area of growing concern in chemical protection is the hardening of delicate electronic hardware. An approach under consideration is the use of conformal coatings to protect circuitry from chemical attack. Military Specification Mil-I-46058C deals with coatings that are approved for use on military printed circuit assemblies. Those compounds that are acceptable for use under this specification are "acrylic, epoxy, silicone and polyurethane resins, and the parylene family of polymers.

Under this specifications, coatings are qualified according to criteria such as materials compatibility, fungus resistance, insulation resistance and thermal shock. The specification does not address the problem of exposure to chemical agents or decontaminating solutions.

ARMY REGULATION AR 70-71

U.S. Army adopted Regulation AR 70-71, published in April, 1984, addresses the contamination survivability of army material. This document states that systems and

personnel must be able to "withstand a nuclear/biological/chemical (NBC) contaminated environment without losing the capability to accomplish the assigned mission".

The regulation addresses three areas:
1. *Decontaminability* - "The equipment must be capable of being decontaminated using standard NBC decontaminants and procedures available in the field."

2. *Hardness* - "Mission-essential equipment and material shall be hardened to ensure that degradation over a 30 day period of no more than 5 percent in selected quantifiable essential characteristics is caused by five exposures to NBC contaminants and decontaminating procedures in the field."

3. *Compatibility* - "The equipment must be capable of being operated, maintained and resupplied by personnel wearing the full NBC protective ensemble."

Specialty Coating Systems, Inc. has conducted simple exposure tests with a number of candidate coatings to determine the effect of chemical agents on various coatings.

SELECTED TEST AGENTS

Tests involving the use of actual surety agents or analogs can only be conducted in authorized field testing facilities or by the military. There are only about a dozen facilities in these categories and tests costs are about twice normal procedures. The subject labs are very busy and it is difficult to accomplish testing.

For these reasons the company decided to limit testing to the most commonly used decontaminating agent, DS-2. This compound is less dangerous to handle and was available to the company because of the voicemitter project mentioned earlier.

DS-2 is highly corrosive and highly toxic. The principle active agents in DS-2 are diethylenetrimine and sodium hydroxide. The material also contains ethylene gylcol-monomethylether. It attacks and corrodes some metals such as cadmium, tin, zinc and aluminum. It will attack plastics such as mylar, lexan, polyvinyl chloride, cellulose acetate and acrylic. It will also attack paint, wool and leather, as well as oxidizing materials.

TEST DESCRIPTION

Standard glass/epoxy coupons with "Y" shaped copper conductors were selected, as specified in Mil-I-46058C (Figure 3). The glass/epoxy substrates were coated with samples of each of the five coatings allowed under the military specification.

Leads were attached to each coupon, and they were immersed to 2/3 of their lengths in full strength DS-2 in individual containers (Figure 4). Leads were connected to a precision ohmmeter set at 100KΩ. DS-2 is a highly conductive material, and as such

will cause the measured resistance value to drop as the protective coating fails, thus allowing conduction of current across the 0.030 gap between circuit traces.

The test patterns were monitored at 15 minute intervals for evidence of failure by both visual inspection and measured resistance. After electrical failure occurred and was recorded the coupons remained immersed in DS-2 to determine cumulative effect on the coatings.

TEST RESULTS

The first test coupon was coated with a durable UV epoxy resin, which failed the ohmmeter test after one hour and 40 minutes exposure. Continued immersion demonstrated that the coating was completely soluble in DS-2 (Figure 5).

The second coating tested was an acrylic resin. This coating began to exhibit evidence of failure after eleven hours of DS-2 exposure. Blackened corrosion spots became visible on the conductor traces under the coating, showing that DS-2 was migrating through the coating (Figure 6). After 24 hours the coating completely separated from the test board (Figure 7). This material is resistant to DS-2 but is partially soluble or permeable after prolonged exposure.

Next to be tested was a polyurethane coating that failed the ohmmeter test in less than 30 minutes. This material dissolved with continued exposure, leaving a white oxidate residue (Figure 8).

The fourth material tested was a silicone resin. This formulation also failed in less than 30 minutes, showing delamination and solubility on exposure to the decontamination solution (Figure 9).

The fifth and final material to be immersion-tested in DS-2 was parylene "C". This coating withstood direct exposure and was still intact after six months when the test was halted. Removal and visual inspection showed no effect on the appearance or functionality of the coating.

These test results are consistent with those obtained at the Army Materials and Mechanics Research Center, where conformal coatings were immersion tested on various types of transparent plastics. Only parylene was found to be completely inert to this chemical compound.(Ref. 6)

Total chemical immunity to DS-2 is, however, dependent on achieving and maintaining coating integrity. Scratches and abrasion can lead to localized attack on plastic substrates (Figure 10). Other coating types show a tendency to delaminate once physical damage to the coating occurs. Agent enters at the damage point and the clear substrate, resulting in delamination of the coating and fogging and/or crazing of the plastic substrate.

Figure 11 shows a magnified view of a polycarbonate test strip coated with 12.5 microns of parylene C. The coating was then scratched with a "cross-hatch" pattern and immersed in DS-2. As the micrograph shows, damage has been confined to the area immediately surrounding each scratch and no delamination hazing or crazing has occurred. Tests show that thicker coatings provide more protection from mechanical damage and are very effective in localizing erosion of the coated substrate.

The non-fogging, non-crazing characteristics of parylene can be important in gas mask lens systems and various other clear shielding situations (windows, canopies,etc.).

CIRCUIT BOARD TEST

As a further test of the effects of DS-2 on electronic assemblies a circuit board immersion test was conducted. Two similar circuits were prepared, one coated with 25 microns of parylene "C". The second was no coated and served as a control unit. Both of these samples were completely immersed in DS-2 for a period of one week.

Upon removal the parylene-treated board was completely unaffected while the uncoated board had suffered serious damage, sufficient to result in a field failure (Figure 12).

Flat capacitors had crumbled (Figure 13), the transistor and IC housings had been eroded (Figure 14). apparently DS-2 attacks certain types of matrix materials in composites. Fibers are left intact, but the matrix holding them together is dissolved (Figure 15). Relays were also attacked and LEDs were frosted. Time studies also show that failure to completely remove the DS-2 can result in latent corrosion (Figure 16). this is a clear demonstration that unprotected electronics are at great risk in the chemical warfare environment.

SUMMARY CONCLUSIONS

Of the five families of polymer: acrylics, epoxies, silicones, polyurethanes and the poly-para-xylylenes, only the latter demonstrated true hardness to decontaminating solution DS-2. There are currently more than 80 coatings on the qualified product listing (QPL-4) for Mil-I-46058C. While not all of these materials were tested, they fall under the four categories whose basic chemical structure makes them susceptible to attack by these agents.

The backbone of the poly-para-xylylenes is entirely composed of carbon atoms. It is this structure that is thought to contribute to the extreme inertness of this family of polymers (Ref. 3). This preliminary investigation on the chemical warfare resistance of conformal coatings is not intended to be a complete and definitive work. It is hoped that this brief study will serve to stimulate further investigation into the chemical hardness of conformal coatings currently in use.

The chemical hardness of the poly-para-xylylenes has been established through testing and actual NBC applications. The barrier properties of parylene are well-known and documented, and the technology has been well established and refined over the decades since the material was first commercialized.

The potential benefit of parylene technology to the field of NBC survivability cannot be ignored and promises to provide a new range of alternatives for retrofit protection of field equipment as well as equipment under design.

The development of new technologies as well as the proper use of existing technologies serves to place new tools in the hands of the military establishment that will enable them to better address the extremely complex challenges of NBC exposure as directed by AR 70-71.

REFERENCES

1. Military Specification Mil-I-46058C
   UCA Eradcom - Delet-R-S.
   Ft. Monmouth, NJ 07703-5302
2. Army Regulation AR 70-71
   Headquarters, Department of the Army
   Washington, DC
3. "Poly-Para-Xylylene, Its Chemistry and Application in Coating Technology,"
   Polymer Engineering and Science, July, 1976, Vol 16, No. 7.
4. Qualified Product List Q.P.L. 46058.39
   U.S. Army Electronics - Research and Development Command
5. U.S .Navy SECNAVINST 3400.2
6. Chemical Warfare Testing of Electric Systems, Per DAAH01-84-D0005, 8/1987
   Dr. James Pfau
7. U.S. Air Force Regulation 80-38

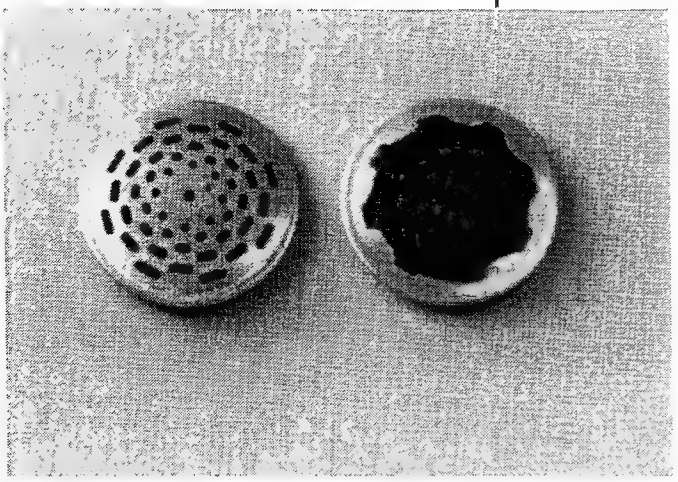


Figure 1. - Parylene protection of voicemitter mylar diaphragm.

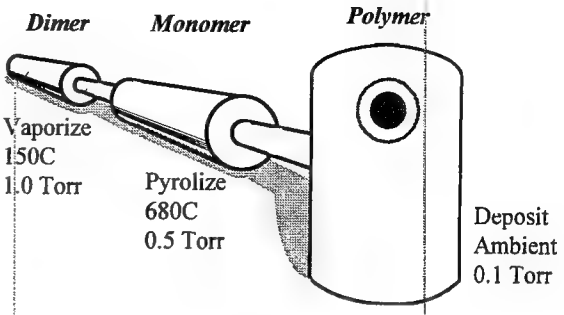


Figure 2. - The parylene vacuum deposition process.

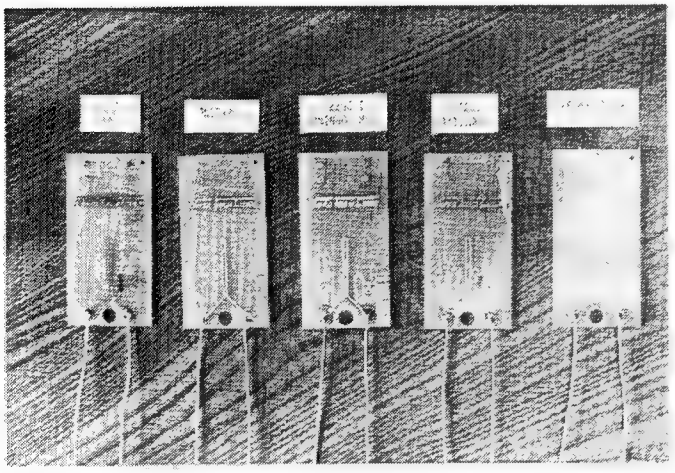


Figure 3.- Test coupons with various conformal coatings (L to R, UV, epoxy, acrylic, silicone, parylene, polyurethane).

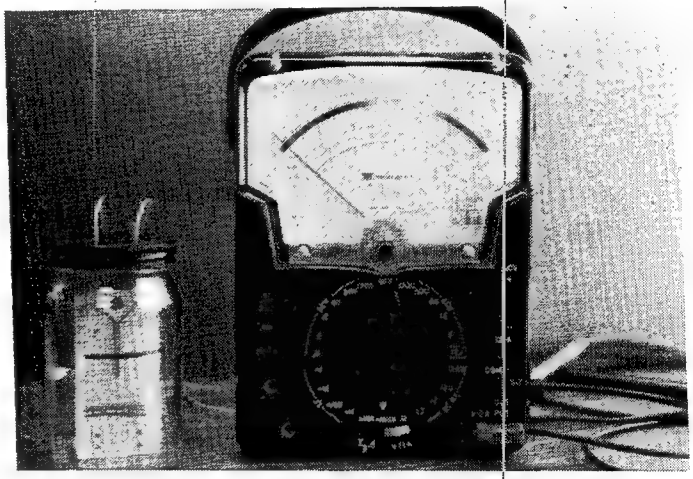


Figure 4. - Resistance testing of immersed coupons.

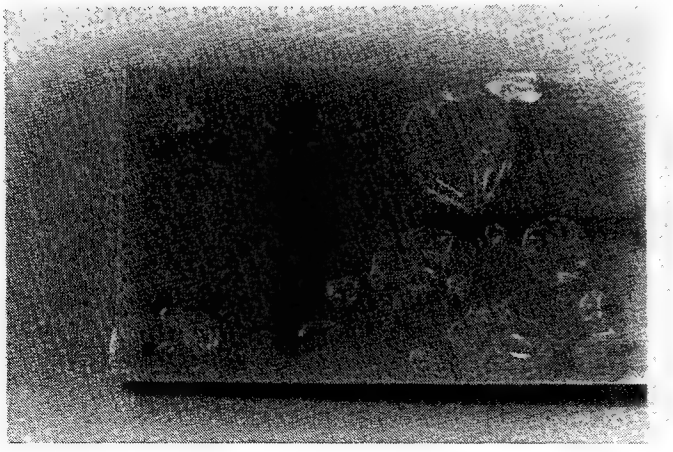


Figure 5. - Rupture of epoxy coating after DS-2 exposure - 100 min.

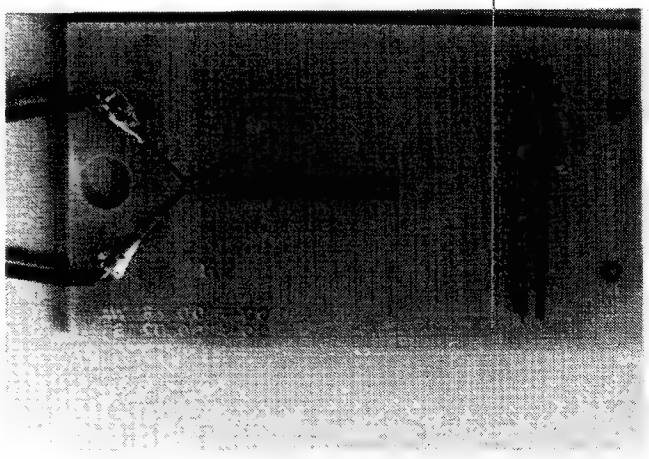


Figure 6. - Spot corrosion on acrylic coating after DS-2 exposure - 11 hrs.

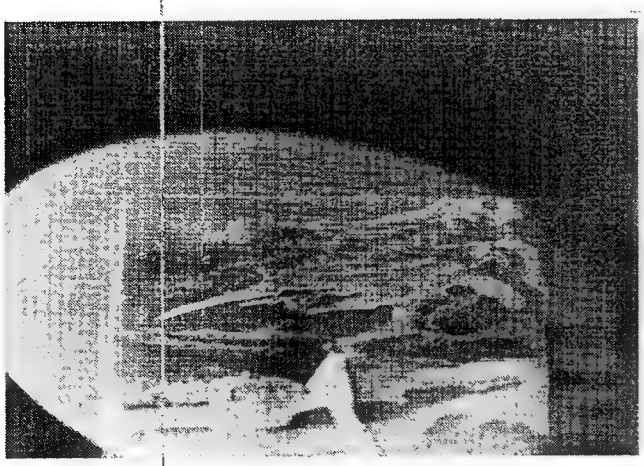


Figure 7. - Total delamination of acrylic coating after DS-2 exposure - 24 hrs.

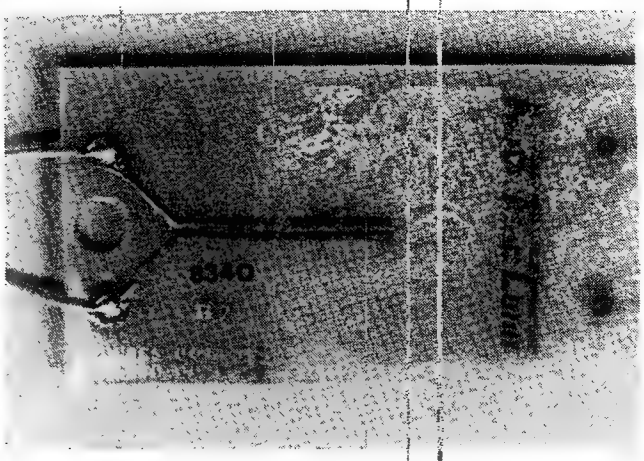


Figure 8. - Massive oxidation of polyurethane coating after exposure to DS-2 for six hrs.

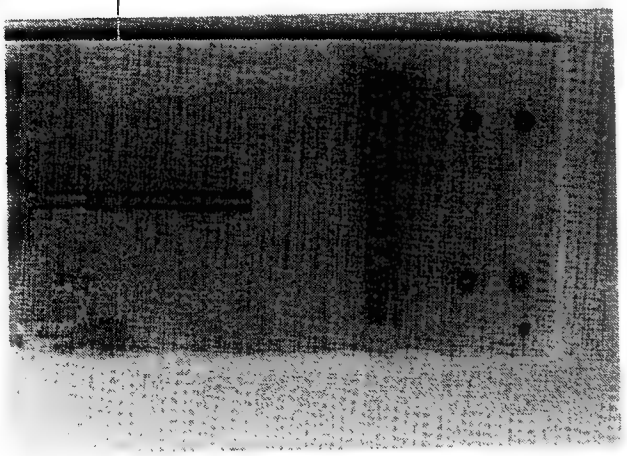


Figure 9. - Erosion and rupture of silicone coating after DS-2 exposure - less than 30 min.

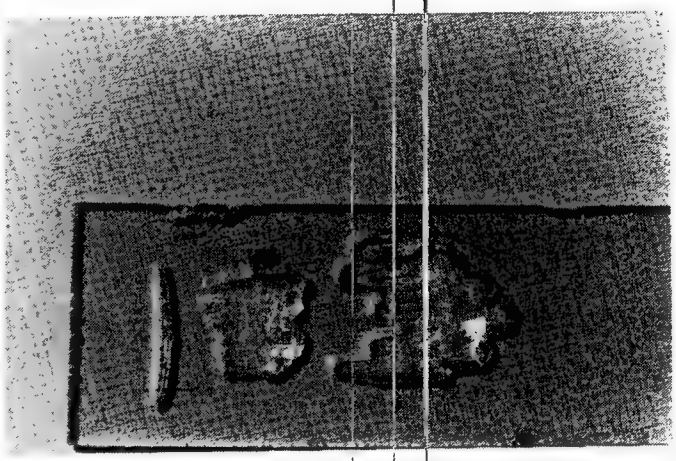


Figure 10. - Eroded polycarbonate sheet after DS-2 exposure and scratch test - 2 hrs.

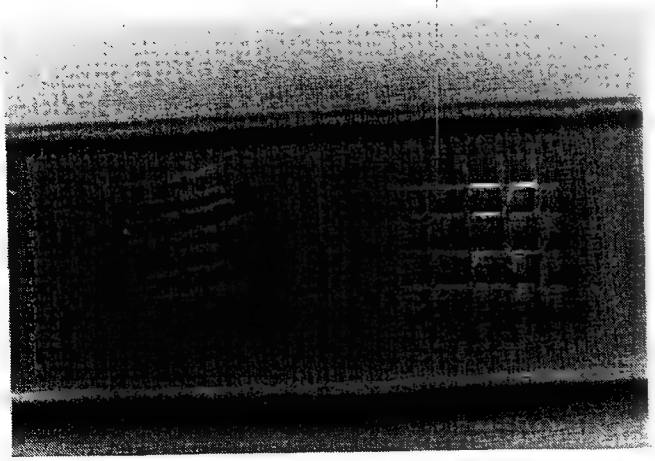


Figure 11. - Localized erosion of parylene-coated (12.5 microns) polycarbonate sheet was confined to scratch area.

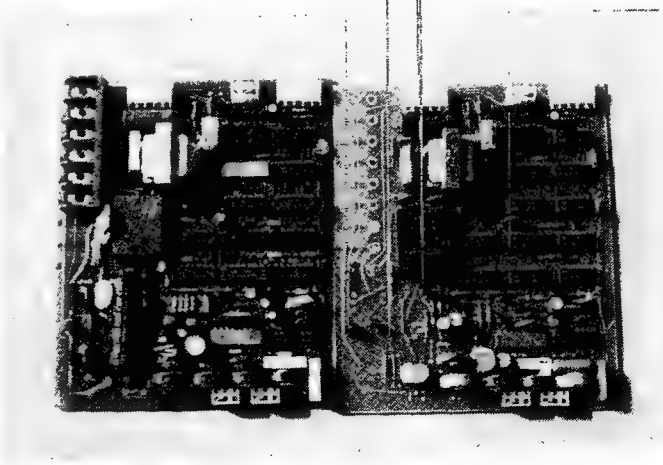


Figure 12. - Parylene coated circuit board (left) uncoated circuit board (right) after DS-2 exposure - one week.

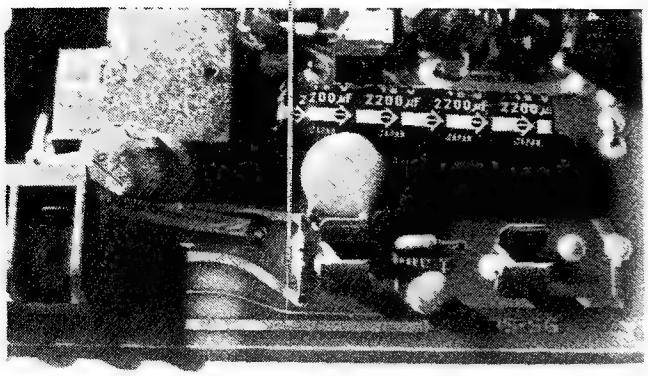


Figure 13. -Damaged flat capacitor on uncoated board after DS-2 exposure - one week.

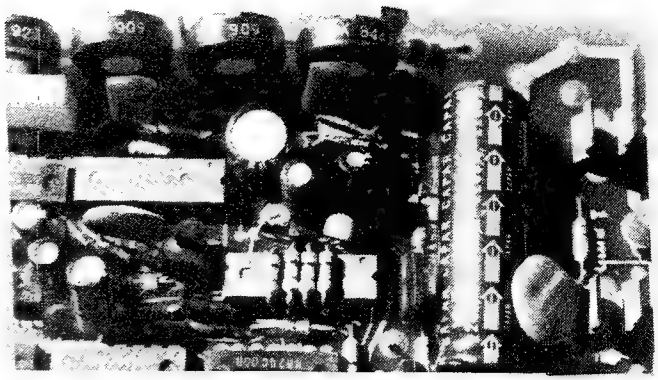


Figure 14. - Transistor package on uncoated board eroded after DS-2 exposure for one week.

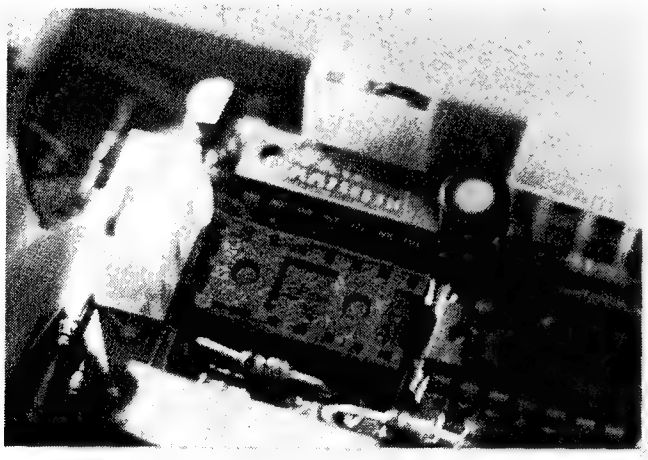


Figure 15. - IC socket on uncoated board eroded after DS-2 exposure for one week.

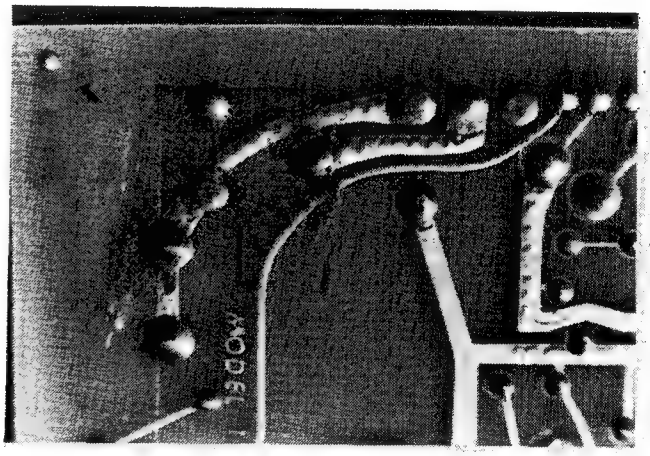


Figure 16. - Latent corrosion of circuit board traces resulting from incomplete decontamination.

Roger Olson is Director of Technology and New Business for Specialty Coating Systems, Inc., a subsidiary of Alpha Metals, Inc.

He has been involved in the conformal coating industry for 23 years and is the author of numerous articles and publications.

He has a degree in electrical engineering from the Milwaukee School of Engineering.

Address: Specialty Coating Systems, Inc.
5707 W. Minnesota Street
Indianapolis, IN 46241

Proceedings paper not available at time of publication.

John Fischer heads the Chemistry and Materials Branch at the Naval Air Warfare Center Weapons Division (NAWCWPNS) China Lake, California. He has 8 years' experience as a research chemist and 4 years' experience in soldering technology.

Address: Naval Air Warfare Center Weapons Division
Code 474200D
China Lake, CA 93555-6001

THE SEARCH FOR CFC ALTERNATIVES IS OVER?

by

Tim Crawford
Project Leader
Electronics Manufacturing Productivity Facility
Indianapolis, Indiana

ABSTRACT

The Electronics Manufacturing Productivity Facility (EMPF) is a U.S. Navy Center of Excellence tasked to do research in electronics manufacturing. For the past seven years, the EMPF has performed extensive research on various cleaning materials and processes that have recently been made available to printed circuit board assemblers. This paper outlines our research and points out the positive and negative aspects that need to be considered when choosing an alternative process.

INTRODUCTION

The search to find suitable alternatives to chlorofluorocarbon-based (CFC) cleaning solvents is coming to an end. That does not mean the issues are any clearer, nor does it mean the decisions are any easier. It means that we are out of time and a decision, right or wrong, has to be made.

The Electronics Manufacturing Productivity Facility (EMPF), located in Indianapolis, Indiana, utilizes information learned from research and disseminates it to the electronics manufacturing industry via final reports, technical articles, seminars, and workshops. Part of our charter is to give telephone consulting to those who have problems in specific areas of their assembly process. Many of the telephone inquiries that I have received lately usually begin, "I heard that CFC's are being phased out. Is this true?" Or, "My boss told me to get rid of our CFC's. What other solvent can I put in my vapor degreaser?" "I heard CFC's are being phased out, but I'm just going to have to get a waiver because I still need to clean." There was one caller who proudly stated "I don't know what all the fuss is to get rid of CFC's. I found a solvent that works just fine. Trichloroethane!" It was hard to tell him that he had jumped off a sinking ship into a life raft with a big hole in it.

For those who are still unsure of the situation, here it is in a nutshell. Scientists have claimed (whether you agree with them or not) that CFC molecules are depleting the Earth's

protective ozone layer. In 1987, the Montreal Protocol was signed, calling for a gradual global reduction of all production of CFC's by the year 2000. President Bush accelerated the reduction to include a complete phaseout in the United States by 1995. Shortly after that, the Copenhagen amendment adopted that same phaseout for the rest of the world. DuPont, the world's largest producer of CFC's, has announced it will stop all Class I CFC production by the end of 1994. In an effort to dissuade manufacturers from using CFC's, the Clean Air Act established a labeling law effective May 15, 1993, requiring products made with, or containing, Class I or Class II CFC's be labeled as such. As an added burden, annual tax increases imposed by the federal government are driving the cost of CFC's higher each year.

If you are one of many who are thinking, "No problem - I still have a whole year," there is more. Consider that even if you had complete control of your budget with unlimited financial resources and were able to order equipment today, you should not expect delivery for 6 to 12 months depending on how many other orders were taken that day. Add to that the acquisition of water treatment systems (both before and after the cleaning process), an air treatment system, installation, process development and training; all of a sudden a whole year does not seem that long.

Before any of this can happen, of course, you must select from the many cleaning chemistries and alternate fluxing/soldering processes that are available. You could call various vendors and listen to their sales pitches, or sift through junk mail and look for the advertisements with water falls, green grass, sunshine, smiling birds, orange trees, and the all too familiar universal symbol for "contains no CFC's". Selecting a substitute that is right for your process is a job in itself, and you can't take short-cuts by looking at your neighbor's house to see what they're using. What's right for their process may or may not be right for yours. The cleaning efficiency of a solvent will depend on variables such as flux type, board design, density, component types, throughput, cleaning machine, time, spray nozzle configurations and pressures to name a few. In addition, environmental laws vary from state-to-state and even between localities.

CFC ALTERNATIVE TESTING

The EMPF, along with the Institute for Interconnecting and Packaging of Electronic Circuits (IPC), has tested 15 commercially available solvents to date (see table) for use with rosin-based fluxes. Although these solvents have passed a very carefully controlled test, the "best" solvent or even "possible" solvent will vary with your process. You may use this list as a starting point, select a few possibilities, and see what works best for you.

In addition to deciding what works best from a cleaning standpoint, there are other concerns that must be considered. Material compatibility examines how these cleaning

materials will react to materials on your product such as part markings, solder mask, laminates, and some components. Industrial hygiene and safety addresses odor, flammability, and exposure limits. From an environmental standpoint, is the waste treated as hazardous material or can the solvent be easily treated to drain, recycled or even close-looped. Considering the trend for cleaning the environment, is your alternative a volatile organic compound (VOC) or a global warmer that may be next on the chopping block. Finally, the cost associated with the new process needs to be considered: equipment costs, material costs, operational costs, maintenance costs, engineering, labor and training costs. There are also costs associated with support equipment for water, air, and waste management.

PHASE 2 APPROVED CFC ALTERNATIVE CLEANING MATERIALS
AS OF NOVEMBER 1, 1994

Allied Signal Genesolv 2004	Mike Ruckriegel	(201) 455-6751
Alpha Metals 2110	John Stevenson	(201) 434-6778
British Petroleum Prozone	Dave Dodgen	(214) 238-1224
Bush Boake Allen Solvent E212	Richard Lamp	(904) 783-2180
Church & Dwight Armakleen E-2000	Frank Cala	(609) 683-7068
Dr. O.K. Wack Chemi Zestron	Karsten Lessmann	011 49 841-635-0 (Germany)
ECD Emulsonator/DuPont Axarel 36	Steve Glass	(503) 659-6100
Exxon Actrel ED11 & Actrel ES	Jim Schreiner	(713) 425-2115
Envirosolv KNI-2000	Steve McCane	(904) 724-1990
Hughes RADS	Rick George	(310) 616-6085
ISP Micropure CDF	Jim Butler	(201) 628-3345
Kyzen Ionox MC	Kyle Doyel	(800) 845-5524
Petroferm Axarel 32	Jim Scott	(904) 261-8286
Petroferm Axarel 38	Jim Scott	(904) 261-8286
Petroferm Bioact EC7	Craig Hood	(904) 261-8286
Petroferm Bioact EC7R	Craig Hood	(904) 261-8286
Petroferm Bioact EC-Ultra	Craig Hood	(904) 261-8286
Petroferm/3M Advanced Vapor Degreasing		
Petroferm Solvating Agent 24	Christine Fouts	(904) 261-8286
3M PF-5070	Wayland Holloway	(612) 737-3030

In addition to the solvents listed, other cleaning processes are either in process or being planned for the near future.

CLEANING WITH ULTRASONIC ENERGY

Using ultrasonic energy to satisfactorily clean tough situations or improve a less-aggressive solvent's cleaning ability may also be an option. Historically, the military has been against the use of ultrasonics because of some studies performed in the 1950's that showed ultrasonic frequencies were causing fragile wire interconnects between the die and the

terminal of microelectronic devices to vibrate enough to fatigue and eventually break. The military has recently changed its stand however, and the latest revisions to some military specifications now state:

> *"Ultrasonic cleaning is permissible on electronic assemblies with electrical components, provided the contractor has documentation available for review showing that the use of ultrasonics does not damage the mechanical or electrical performance of the product or components being cleaned."*

This change of heart by the military is due to more recent studies conducted by the EMPF and other research laboratories that have given us a better understanding of ultrasonics. At the same time, newer wire bonding techniques have provided a more robust component which is more able to withstand the harsh vibrations of ultrasonic energy. This is not to say ultrasonics is 100% safe. Under proper conditions, ultrasonics can be a useful tool, but fatigue is a part of life with ultrasonics, and some components under certain applications will fail. "Test clean" a safe sample of your product using ultrasonic energy before you invest a large amount of time or money.

WATER SOLUBLE FLUXES

Another option may be to eliminate rosin-based fluxes all together and use a water soluble flux (WSF). WSF can be cleaned either by using water alone, or water with a detergent/saponifier. WSFs will typically provide excellent solderability and enlarge the soldering process window. The reason they provide such good solderability is because of their corrosivity; however, these corrosive properties can cause problems if cleaning is not properly performed. If a WSF were to get trapped in an area such as under a tightly spaced component, inside an unsealed component, or up under the insulation of a stranded wire, a failure is likely to occur. Many WSFs contain polyethylene glycols and other polyglycols which are nonionic and hygroscopic; meaning they will absorb moisture from the air and promote electrochemical migration and degradation of electrical performance in the presence of ionic contamination. Since polyglycols are nonionic, they cannot be measured in the commonly used resistivity of solvent extract cleanliness tests such as the Omegameter™ or Ionograph™. Recent revisions to military specifications are allowing the use of WSFs (except on stranded wires and unsealed components) with certain restrictions being placed on those containing polyglycols. These restrictions are currently being reviewed by the Navy.

LOW RESIDUE FLUXES

If selecting a cleaning process looks tough and you're thinking about taking the easy way out by going to a low residue or "no-clean" flux, it's not that easy. No-clean does not mean you do not have to clean because there is no residue; it means you do not have to clean because the residue is small and not detrimental to the assembly. Low residue (LR) fluxes, also known as low solids or no-

clean fluxes, were formulated to leave a minimum quantity of a benign residue. This residue is not conductive or corrosive; however, it may interfere with the adhesion of the conformal coating. As in choosing a cleaning material, other issues must be considered when selecting and implementing a low residue flux. Material compatibility, environment, industrial hygiene, safety, and cost associated with the new process all need to be considered. Flux application is not as simple as it was with the good old rosin-based fluxes, and the operator must have an intimate knowledge of his soldering process. On the positive side, the military recognizes the potential for using LR fluxes for a broad range of soldering applications, including soldering of stranded wires and unsealed components. The potential of LR fluxes is reflected in the most recent revisions to military specifications.

In contrast with the WSFs, LR fluxes are not very aggressive, therefore they create a smaller soldering process window. This window can be enlarged by using an inert atmosphere such as nitrogen to reduce oxidation of the base metals. Another process worth considering, which also requires nitrogen, uses a dilute adipic acid to precondition the board. The actual soldering takes place in a sealed chamber filled with an inert atmosphere of nitrogen and formic acid. When exposed to the high temperatures associated with wave soldering, the adipic acid evaporates and the formic acid converts to carbon dioxide and water. Only a small amount of noncorrosive residue is left on the assembly.

Manufacturers who are going to LR fluxes with the intent of not cleaning must think no-clean ***process*** from incoming component and board cleanliness levels throughout all stages of handling, processing and shipping. Implementing a no-clean process is not as simple as changing the flux and rolling the vapor degreaser out into the back alley for the trash collector. Unfortunately, flux is not the only source of contamination. There are several very ionic, very corrosive materials that are used in the manufacturing of bare boards. An assembler must verify that the bare boards, along with components and other parts to be used on the assembly, are clean upon receiving, then maintain that level of cleanliness throughout the assembly process. Ionic and nonionic residues come from many sources and preventing this contamination from coming into contact with the assembly is hard. Even a bare board that was verified to be clean upon arrival at the assembly facility may still leach ionic materials when exposed to elevated temperatures. Parts are sometimes stored for months at a time in a clean(?) storage area awaiting subsequent operations. Depending on the environment (temperature and humidity), solderability will decline with time and may become unsolderable with a less aggressive flux. A good first-in/first-out system is important. Boards are handled and moved from station to station for component insertion and soldering. The cleanliness level of the parts is only as clean as the people handling them, and many people do not realize that not all gloves are free of ionic residue. If the gloves are free of ionic residue, do assemblers contaminate the outside of the gloves when removing them from the bag or when putting them on? Will an assembler use the gloved hand to open a valve, turn an unclean doorknob, or satisfy an itch? A no-clean process is possible, but it starts from the bare board and continues until the assembly is complete. There are big companies, with big research departments and big dollars that have spent years developing a reliable LR process.

CONCLUSION

Choosing and implementing a process that is right for your particular assembly house takes time, and you have no time-outs left. CFCs will be phased out by the end of 1995. Acquiring CFCs will be harder and even more expensive in 1995, and the labeling law is currently in effect.

- Will you use rosin-based, water soluble, or low solids flux?
- Will you solder in air or nitrogen?
- Which solvent is best?
- Which machine is best?
- Which process is best, aqueous or semi-aqueous? Batch or in-line?
- Should you use ultrasonic energy?
- Will you recycle, treat or close-loop your effluent?
- Will you clean or is no-clean the ultimate solution?

A decision has to be made because the search to find suitable alternatives to CFC-based cleaning solvents is coming to an end!

Tim Crawford is a Project Leader for Electronics Manufacturing Productivity Facility (EMPF) with more than 9 years' experience in various aspects of the manufacturing process, focusing primarily on cleaning and cleanliness testing.

A member of IPC, he is vice-chairman of the Acoustic Energy Cleaning Task Group and co-chairman of the Ionic Cleanliness Testing Task Group. He received the EPA Stratospheric Ozone Protection Award in 1993.

He has an A.A. degree from Cerro Coso College, Ridgecrest, California.

Address: Electronics Manufacturing Productivity Facility
714 N. Senate Avenue
Indianapolis, IN 46202

IMPLEMENTING A SUCCESSFUL SPC PROGRAM AND USING PROCESS CONTROL STUDIES IN THE ELECTRONICS INDUSTRY

by

Moin Ansari
Manager Continuous Improvement, SPC and Training
Scientific-Atlanta, Inc., San Diego, CA

ABSTRACT

Statistics has been in existence since time immemorial. industry. Since the backbone of U.S. manufacturing was in Detroit, the early implementation of Statistical Process Control (SPC) was conducted in the automobile most. Most of the literature on SPC is for *Variable Data* as it is applied in the heavily mechanized automobile industry or their suppliers. In many cases the costs of measuring variable data does not justify application of SPC in the electronics industries.

Implementing Statistical Process Control in the Silicon Industry is a fairly new phenomenon. There are very few texts that deal with SPC in the Service and/or Electronics Industry, and the information that does exist is vague and does not do justice to the subject. Many believed that the electronics or service industries could not take advantage of the control charts.

Thanks to the persistent efforts of many Japanese companies, new Statistical techniques have been developed within the past few years. SPC for this decade is significantly different than SPC of the Eighties. As a result of the new techniques, the Nineties have seen a dramatic proliferation of Statistical Techniques into the Electronics sector. New industries have just begun to utilize statistical tools using attribute data. Motorola has been a torch bearer in the field.

Scientific-Atlanta, Inc. (NYSE:SFA) is a Fortune 500 Company with divisions in San Diego, Canada, Mexico, Phoenix, and Atlanta. We are a world leader in Broadband communications systems, satellite-based communications networks, and instrumentation for industrial, telecommunications and government applications..

We have achieved dramatic gains in productivity and First Pass Yields by implementing a cradle to grave Statistical Process Control system. To keep our costs down, to remain competitive, and get an edge over our competition, Scientific Atlanta places heavy emphasis on monitoring our manufacturing processes closely through SPC. Our Process Action Teams take Corrective Action on the problems to reduce non-value added activities like scrap and re-work. We use the latest Statistical techniques to Benchmark our defects to the industry best and strive to achieve part per million defect rates.

To simplify data collection, eliminate data entry errors, and have to have real-time data available for analysis, our operators use our automated, bar-coded, state of the art, computerized SPC network. The entire factory floor has designated SPC nodes (data collection points). The nodes have dedicated 386 or 486 PCs and bar-code input systems. The SPC nodes are networked through a Novel Local Area Network (LAN). All data collection PC nodes are linked to the SPC coordinator.

This paper is a case study in implementing a successful SPC program in an Electronics environment. The paper will cover data collection, control-charting, process capability studies, part per million calculations, six sigma concepts, inspection elimination and corrective action.

DEFINING SPC

Statistical Manufacturing Control (or Statistical Process Control as it is generally called) is the application of statistics to manufacturing to analyze processes and keep track of products. Statistical Process Control is the Application of statistical techniques to instigate process control. Today SPC is used in both the manufacturing and service industries.

Some think that SPC is the process of producing products within tighter specifications. Nothing could be farther than the truth. Many consulting enterprises have cheapened SPC by selling it as TQM. SPC is a discipline anchored in statistics and mathematics. SPC implementation banks on Total Quality tools to improve systemic problems within the corporation or government process.

There are many buzz words out there. SPC is not one of them. This paper is an attempt to explain the basics of SPC. Statistical Process Control is a body of knowledge that can be used in very diverse circumstances. The employees gather data, and display it in a manner that makes sense to the people who are working with it. The Data is used to take appropriate Corrective Actions.

Most manufacturing industries are capable of applying SPC systems. Many service industries are applying SPC techniques to improve themselves, and their processes. Statistical Process Control is a systematic method of tracking, predicting and minimizing product characteristic and process variations. If variation is the archenemy of production and/or services that are produced, then the SPC helps in the following:

1) Reduce costs
2) Increase quality and yields
3) Discover hidden and latent engineering and process design problems
4) Decrease Cost of Quality: Scrap, Rework, and Wasteful inspection
5) Identify sources of process and product variation
6) Solve difficult problems involving specs and requirements
7) Monitor trends, and take Corrective Actions ahead of time

SPC has two components, Control and Capability. Both these components have to be established to get meaningful results. Capability has to be established after the process has been brought under control. After the process is in control and is capable, we turn to sampling plans to assist us. All of these definitions will be explained in this paper.

THE HISTORY OF SPC

Beginning with Paleolithic man, humans have been improving processes to find the optimum way of producing articles. Process control has been extensively used in the production and crafting of weapons for hunting and warfare. Fred Flickstone was using SPC (without the charts) to find the best way of producing arrowheads. Once the best arrow was tested this optimum arrowhead was standardized and proliferated throughout the tribe. The process of manufacturing arrowheads was brought in control. It is amazing that arrowheads found in America used by native Americans are almost exactly the same size and shape as the ones used by Australian aborigines, and African tribesmen. The wheels of schooners heading out to conquer the American wild west in the new world are almost the same shape as the wheels on bullock-carts in India (used even today!).

Statistics have been used throughout the ages to define a process and then standardize it. Walter Shewhart "invented" the control chart while working on headphones at AT&T Bell Labs. He wanted to find out the variation in head sizes.

After General Macarthur had conquered Japan, he wanted to establish the new industry in Japan on solid mathematical grounds. Shewhart was invited to Japan but he could not make it there. Edward Deming and two unknown gentlemen by the name of Homer Sarasohn and Charles Protzman went to Japan and set up SPC in many of the industries. Sarasohn was made chief of the Industry branch within the Civil Communications Section , tasked with building the communications setup in Japan. Protzman was in charge of the Japanese telephone system. Edward Deming is the best known American who was instrumental in making the Japanese industry so very competitive.

Around the eighties America discovered Deming and SPC. Most of Deming's methods were tried in the automobile industry in Detroit. Most of the Statistical methods are anchored in heavy machining methods. In the mid-eighties American service and electronic industries began using SPC in an efficient manner. Motorola and others are the vanguard of the SPC revolution in America. Today modern research allows us to truly utilize SPC in the electronic industry.

IMPLEMENTING SPC AT SCIENTIFIC-ATLANTA

Many electronic industries have achieved dramatic successes in their manufacturing areas. The following article was published in the Scientific-Atlanta Quality Newsletter:

Laser wands and bar codes, colorful PC displays and electronic messages are eliminating the cumbersome information paper trail that was once a way of life in manufacturing at Scientific-Atlanta.

Through the use of a process called Statistical Process Control (SPC), manufacturing managers can access information in seconds that may have taken hours or days a year ago.

Moin Ansari, Manager of continuous improvement, SPC and training programs at Signal Processing Systems Division in San Diego is responsible for directing the paperless flow of information that keeps the Sad Diego facility's manufacturing site humming.

"All of our work stations are connected to each other through PCs and interactive Local Area Networks", Ansari explained. At each station we can call up reports about what work is being done and within seconds view in chart form the progress of the manufacturing process. We can see if any defective parts have been discovered in the manufacturing process and trace their origin to the supplier and initiate corrective action.

" In addition, we can produce trend analysis in our manufacturing based on the work in process so we can adequately predict our requirements for the future".

SPC is being introduced throughout the company's manufacturing centers, with all business functions to follow. The manufacturing sites will incorporate the program by the end of the fiscal year. The SPC program has been championed by the Quality Council to proliferate throughout the company as a way to ensure uniform processes in manufacturing and production of the highest quality products.

The benefit of having Statistical Process Control in our manufacturing process, "Ansari added, " is to make us a more flexible manufacturer and more competitive in the marketplace."

ECONOMIC BENEFITS OF A COMPUTERIZED SPC PROGRAM AT SCIENTIFIC-ATLANTA, SIGNAL PROCESSING SYSTEMS DIVISION (SPS), SAN DIEGO

The following article was published in the Scientific-Atlanta, Instrumentation Group Newsletter:

> *The SPS Division in the road to World Class Manufacturing. The division is using computer systems in manufacturing to become a leader in the industry. To keep costs down, and to reduce scrap and rework at a minimum level, the Manufacturing Operations decided to invest in a system that would provide essential information to management. We have installed a state of art computerized Statistical Process Control (SPC) data collection and data analysis system that is the envy of the Southern California electronics industry. The system collects data through bar-coding, and feeds the data to PC that are networked throughout the manufacturing facility. The network also is capable of displaying manufacturing aids to the operators. Live drawings can also be piped into the system. Voice and multi-media presentations will be an integral part of network. Videos on soldering etc. would be available to the operators on demand. Going paperless is one of the division goals. The network will assist the manufacturing engineers in providing paperless Routers to the system. On-line, real-time data is now available, and can be analyzed to discover trends and keep costs down.*

IMPLEMENTING PROCESS CONTROL IN A LEARNING ORGANIZATION

The key to a successful SPC program is education. All the Quality gurus in America, Walter Shewhart, Edward Deming, J.M Juran, Philip Crosby have emphasized the institution of training as a concrete way of controlling processes. Peter Senge in his book *The Fifth Discipline* introduces us to the concept of The Learning Organization. Senge says that "*It is no longer enough for a Sloan, a Watson or a Ford to do all the learning for the entire organization. The organization that will survive in the next century is the Learning Organization where learning is occurring at all levels of the organization*".

Training: Training and education are some of the most important elements of a SPC program. Training should encompass all employees. Some companies have done the following:

a) Basic SPC: 24 hours of SPC training imparted to all involved employees in operations
b) Advanced SPC: 8 hours of SPC training imparted to all involved employees
c) Software training imparted to all involved employees in operations
d) On the Job Training in PATs (Process Action Teams)

Process Control: Edward Deming and Walter Shewhart have proposed the continuous use of Plan, Do, Check, Act (PDCA) cycle to control all process related activities. Elimination of all non-value added activities in the organization is a fundamental principle of quality. Sorting is the process of figuring out which parts meet specifications. This exercise of isolating the variables is called inspection. It is a non-value added activity and costs valuable time and money. Non-value added activities need to be reduced or eliminated through training and SPC. The following gives us a generic plan to bring processes under control:

TABLE 1. The Process Control Cycle

1	2	3	4
IDENTIFICATION	**MONITORING**	**ANALYSIS**	**CORRECTIVE ACTION**
a) Brainstorm Ideas and generate list of problems	a) Select defects to be monitored	a) Identify the potential causes	a) Develop a Corrective Action Plan
b) Define problems using Flow Charts and Requirements Analysis	b) Select/develop performance measures	b) Select likely causes	b) Set Corrective Action objectives
c) Log the defects and barriers (that involve other PATs)	c) Design data collection sheet and graph the data	c) Test likely causes	c) Take Corrective Action
d) Prioritize defects and barriers	d) Select a defect/barrier for analysis	d) Set priority for corrective actions	d) Evaluate the Corrective Action effectiveness

TOOLS FOR A SUCCESSFUL CONTINUOUS IMPROVEMENT SYSTEM

Many tools are used to monitor processes in the manufacturing and service industries. . For further discussion of these techniques please see *The Memory Jogger Plus* (ASQC Press). The tools of SPC are:

TABLE 2. The SPC Tools

The Seven Basic SPC Tools	The Advanced Seven SPC Tools
Brainstorming	Affinity Diagrams
Fishbone, Ishikawa, Cause-Effect Diagrams	Interrelationship Diagraphs
Pareto Analysis	Tree Diagrams
Scatter Diagrams	Prioritization Matrices
Run charts	Matrix Diagrams
Histograms	Process Decision Program Charts
Control Charts	Activity Network Diagrams

Employees use Pareto Analysis to prioritize defects, and Control charts to identify weak processes, and histograms to analyze trends and prevents costly mistakes. Once process is brought under control, capability studies are performed to analyze the capability of processes with respect to customer mandated specifications. Whether we are in the manufacturing sector or the service industry, SPC system will help us improve our short term profits and long term survival by investing in process control.

DATA, INFORMATION AND STATISTICS

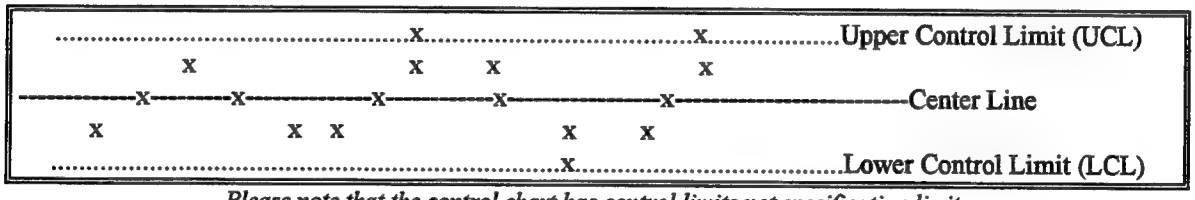
Statistics: It is that arm of mathematics that deals with data collection, data analysis and data presentation. Statistics uses probability and sampling plans to deliver tools to people in the manufacturing and service sectors who want to watch trends.

Data: Data can give us a lot of information if it is properly analyzed. There are two types of data:
Variable Data: Variable data is measurable data, such as pounds, inches and miles.
Attribute Data: Attribute data is subjective, go-no-go type of data that cannot be actually measured.

THE NORMAL CURVE AND THE CONTROL CHART

Normal Curve: The Bell shaped Curve is called a "Normal Distribution Curve" and is a continuous function which means that the curve never ends (it is not "*discrete*"). A Normal Curve is always symmetrical. The Central Limit Theorem states that "*Irrespective of the shape of the universe the distribution average values x-Bar, of subgroups of size n will tend towards a normal distribution.*" That means that regardless of the universe, the average of the parts will always fall in the form of a normal curve.

Control Chart: The Normal Curve is used to plot defects and non-conformities on a graphical chart called a "Control Chart". Each process that is monitored is displayed on this "graphical pictographs" that plots the data on a time-lined chart. These charts are based on hard statistical formulae that assign process parameters to each process. The Statistical "Normal Curve" assigns the normal variation within any process. Variation that falls outside the normal parameters of a process (usually plus or minus three sigma) is identified and appropriate corrective action taken.



Please note that the control chart has control limits not specification limits

Binomial and Poisson Distributions: There are many curves that are available in Statistics. SPC is based on the use of normal and other mathematical distributions. We use the correct curve based upon sample sizes and based upon the types of defects that have to be monitored. For the purpose of control charts we approximate the various curves like Binomial and Poisson to the Normal and use it to do charting. In most cases the Normal curve gives us an adequate approximation.

NORMAL AND ABNORMAL VARIATION WITHIN A PROCESS

Variation is the enemy. Variation between batches and within batches has costs attached to it. Boeing defines Variation as *the arch enemy of Quality*. Boeing has instituted a specification called AQS-D1-9000 on all its 25000 suppliers to eliminate variation. SPC is one tool that reduces and eliminates variation within processes.

Variation: Variation in one or more of the characteristics of a product causes customer dissatisfaction or poor quality.

Motorola believes that "product quality strongly effects manufacturing and engineering cycle times and shipping schedules to name a few. The ability to effectively and efficiently deal with product variation is crucial in achieving six sigma product quality ".

Common Causes: The inherent variation within a process is called common cause variation Control Charts are used to determine the level of variation due to *common causes.* Common causes are a collection of several sources of variation which are inherent to a process such as cold solder, excessive solder, drawbridging, undetected clamping errors, contamination, etc. The collective influence of common cause variation defines the natural process fluctuations. The expected degree of common cause variation is shown by the width of the control limits on a control chart. When the process average stays about the same and the variation about the average also stays about the same level. This is achieved when the process is only being influenced by the common causes of variation.

Process in Control: For any given period of time, a process is usually considered in-control if all plotted points on a control chart in that time period are contained within the control limits.

Process out of Control: The points that fall outside the calculated parameters on a control chart are considered "points out of control". These need to be investigated by using the seven or fourteen tools of SPC. To eliminate the common cause we may have to expend on new equipment

Special or Assignable Causes: Special causes are sources of variation that are not inherent to the process, but can effect it's performance. Control charts are used to identify *special causes.* These special causes can be identified by points falling outside the control limits on an appropriate control chart. The special cause variation is due to a specific cause, such as operator error or shift change. A programming error, or soldering electrical components in the wrong location result in special causes. A frequent cause of special cause of variation is caused by shift changes. Appropriate corrective action will eliminate the "special causes".

TYPES OF CONTROL CHARTS

Variable Data Control Charts

R-chart: Measurement of dispersion used to construct an R-Chart is the subgroup range

S-*Chart:* Measurement of dispersion used to construct an S chart is the subgroup sample standard deviation

X-bar-R chart: Subgroup averages with control limits based on subgroup ranges.

X-*Bar-MR chart*: is derived from an average of the range between successive pairs of observations

Individual: individual performance based on individual readings rather than subgroups

MR-Chart: Successive subgroup averages.

Moving-Average Control Charts: Standard charts are insensitive to small shifts in the average of the process. This is more effective in detecting small process shifts. Like X-Bar-R chart is a plot of subgroup averages with control limits based on subgroup range. Moving range is also a plot of the averages of subgroup averages.

Geometric Moving Average Control Chart: When plotting a point the geometric moving-average control chart takes a weighted average of the current subgroup average and all previous subgroup averages

The Attribute Data Control Charts

P Chart: The percentage or fraction of non-conforming units
U chart: The Average number of defects per unit with a variable sample size
C chart: The average number of defects with a constant sample size
NP chart: The actual number of nonconforming units
Du chart: The number of defects is a u-chart with weights attached to the critical defects

Other Statistical Charts

Yield Charts: Monitor the yields of good boards vs. bad boards in a process
Trend Charts: Monitor the yields, Cp, Cpk, Defects per unit per month/week/day
Histograms and Pareto charts: To identify defects and prioritize them
Correlation charts: To identify correlation between two or more characteristics

CORRECTIVE ACTION EFFORTS IN THE EVENT OF OUT-OF-CONTROL CONDITIONS

Most SPC practitioners use plus minus 3 sigma (σ) as the basis for establishing control limits. Some companies use 2 or 2.5 or 4 sigmas (σ) on each side of the center line. The process may be out of control even if all the points are within the control limits! There are several conventions in assigning "out of control conditions". The following are called "*Western Electric Rules*" developed by AT&T. Many companies modify the rules to suit their particular needs.

1) *Freak*: One random point is out of control
2) *Trend:* Seven consecutive points increasing
3) *Trend:* Seven consecutive points decreasing
4) *Run:* Seven consecutive points above the mean
5) *Run:* Seven consecutive points below the mean
6) *Stratification:* When points may be hugging the center line. Stratification shows us as unnaturally small fluctuations.
7) *Mixture:* If pattern has too many points near the centerline avoiding the control limits
8) *Instability:* If points outside the control limits create a unusual pattern
9) *Instability of shifting process:* If one pattern is repeated on the control chart

If any of the above conditions occur, immediate corrective actions is required. If 2,3,4, or 5 occur process is to be halted immediately and leads and supervisor informed. Immediate Corrective Action should be taken. The process should be sent to a Process Action Team for resolution. The AT&T Quality Control handbook is one of the best sources for Control Chart interpretation (ASQC Press).

Note: Interpreting Attribute Control charts can be an extremely difficult and confusing exercise. The calculation for control limits is based upon the sample size. We must use appropriate sample sizes if we are to achieve process control. The cumulative effects of various defects (if the defects are added up and them charted) in the control charts can be misleading because the totaled defects may show the process to be in control. In Attribute Data Control Charts we need to monitor the individual characteristics separately.

COMPONENTS OF SPC

SPC has two major components. Control and Capability.

Control: Once special causes of variation are eliminated, only common causes remain. This does not mean the process is good or the process is making. It only means that it is consistent and predictable. The

level of common cause variation may or may not be acceptable. An in-control process is consistent but it could be consistently making bad parts! This decision is not made using control charts, but rather with process capability methods which belong to a second aspect of SPC; process capability.

Capability: Determining the standard deviation from the process mean.

TABLE 3. Control vs. Capability

Control	Capability
Differentiates Common from Special causes of variation. Determines process is in control or out of control Control is determined by interpreting patterns on the control chart Control charts are specification independent	*Compares 6 sigmas to Engineering requirements* Common language is Cp, and Cpk, and PPM fallout Requires process is in control BEFORE Cp or Cpk is valid Capability studies are specification DEPENDENT
Control answers the question: Is process changing?	*Capability answers the question:* Is Process always making good parts ?

The results of the two activities depend on each other, yet they are not inter-changeable

SIX SIGMA (6σ)

Standard Deviation or Sigma (σ)*:* Sigma is defined as the variation from the mean (zero, which is the middle of the curve on the x-axis) in a Normal curve. The Normal curve is usually divided into six "segments" (plus and mines three in either direction) or multiples thereof. The "segments" are called "*Sigmas*" (σ).

Statisticians have calculated the area under the Normal curve as follows:

TABLE 4. Three Sigmas

Standard Deviation from Center	Sigmas from Mean	Percentage of Normal Curve
Plus/Minus One Sigma	$\pm 1\sigma$	68.26%
Plus/Minus Two Sigma	$\pm 2\sigma$	95.46%
Plus/Minus Three Sigma	$\pm 3\sigma$	99.73%

MOTOROLA'S DEFINITION OF "SIX SIGMA" (ACTUALLY TWELVE SIGMAS)

Motorola's Six Sigma is a registered trade mark of the Motorola Inc., and is different than the statistical six sigma. Motorola believes that achieving 99% quality is not good enough and has divided the bell curve into twelve segments (plus minus six sigma). Motorola's Six Sigma is actually twelve sigmas.

In addition to the above Motorola has captured the tail of the Normal curve and uses additional sigmas:

TABLE 5. Six Sigmas

Standard Deviation from Center	Sigmas from Mean	Percentage of Normal Curve
Plus/Minus Four Sigma	$\pm 4\sigma$	99.9937%
Plus/Minus Five Sigma	$\pm 5\sigma$	99.999943%
Plus/Minus Six Sigma	$\pm 6\sigma$	99.9999998%

Using Twelve Sigmas instead of the natural plus-minus three sigma

Motorola and many other World Class Manufacturing companies want to achieve a greater amount of quality than the one prescribed by 99.9%. People often think that 95% or even 99% is "good stuff" and is more than acceptable. 99% can actually mean:

TABLE 6. The Meaning of Quality in the Nineties

What does 99% Quality mean	What does 99.99% Quality mean
20,000 lost articles of mail per hour (no comment?!)	2,000 lost pieces of mail per hour
Unsafe drinking water almost 15 minutes each day	Unsafe drinking water per, 1 hour every month
5000 incorrect surgical operations per week	500 incorrect surgical operations per week
2 unsafe landings at most major airports each day	2 unsafe landings at O'hare airport each day
200,000 wrong drug prescriptions each year	20,000 wrong drug prescriptions each year
	50 newborn babies dropped at birth by doctors daily
	Your heart fails to beat 32,000 times per year

To illustrate the concept of Six Sigma (6σ) Motorola asks us to consider the following:

- 1 Electronic System = 20 PWBs (500 solder joints each) = 10,000 solder joints

If only 99% of the solder joints were good, then we could expect 100 joints within each system to be defective. On the other hand, if 99.99966 (six sigma quality) of the solder joints were good, then there would be only 3.4 solder joint defects per 100 systems. When defects are few, quality confidence is high. The difference between six sigma capability (99.99966%) versus 99.0% is a few nines but each nine represents a ten fold reduction in non-conformities. Six sigma quality represents a 2941-fold improvement in quality when compared to a product built under the constraint of 99% capability.

Six sigma (6σ) quality will help in the following:

- Decrease manufacturing and design cycle time
- Improve the ability to accurately forecast inventory needs and cycle time
- Decrease costs due to inventory, scrap and rework
- Increase profitability and market position
- Cultivate new business and hold to old business

Total Factory "Six Sigma" (6σ) defect reduction Program

Mikel J. Harry in *The Nature of Six Sigma* says that "the Six Sigma concept (actually twelve sigmas) is a relatively new way to measure how "good" a product is. When a product is six sigma it tells us that the product quality is excellent. It says that the probability of producing a defect is extremely low. The term "sigma" in quality is a statistical measuring device that tells us how good our products are.

In general when we say that a product is six sigma what we are really saying is that any given product exhibits no more than 3.4 nonconformities per million opportunities (npmos) at the part or process level".

SPC cannot being in the manufacturing sector. SPC begins in the design area. One cannot expect to build to Mil-Std-2000 if the hardware was designed per a basic IPC specification. Harry says that "to help ensure that the typical forms of variation shifts and drifts in the average do not cause excessive differences between and within units of products there are several things that can be done.

1. Designers configure a product in such a manner that its performance is shielded against variation. When designers do this it is known as "designing for producibility".

2. In addition the manufacturer's process(es) as well as that of its suppliers could track down, control, and ultimately eliminate the root cause of variation through the application of statistical process control (SPC) methods, the spread and the centering of the processes can be significantly improved.

3. The Six Sigma (6σ) concept assumes that no two product units can be identical. Some differences will naturally be present; however the differences will so small that for all practical purposes, they will be negligible. In practice, the concept recognizes that very slight variation will be present, but the end result will always be a product that displays excellent quality". These are the various sigma results that are possible":

TABLE 7. Nonconformities Per Million Opportunities = npmo = ppm

Sigma	*Without change*	*With change*
1	317,400	697,700
2	45,400	308,733
3	2700	66,803
4	63	6200
5	.57	233
6	.002	3.4
7	.000003	.019

(Sigma Quality Levels: Before and after 1.5 sigma (σ) change in the average)

Achieving "Six Sigma" (6σ) Quality at Motorola

Mikel J. Harry in The Nature of Six Sigma says that "we must recognize that the product variation results from insufficient design margins, inadequate process control, and less than optimum parts and materials. These the three primary sources of product variation. If we are to achieve six sigma quality, we must isolate, control and ultimately eliminate variation.

We must strive to go beyond just "meeting the specifications". Some of the tools that can help include:

- Short Cycle Manufacturing (SCM)
- Design for producibility
- Statistical Process Control (SPC)
- Supplier SPC (SSPC)
- Participative Management practices (PMP)
- Parts standardization and supplier qualification
- Computer stimulation

Not only do these tools help us remove variation while the product is being built, they can detect the presence of variation before we go into production. In this manner we are able to prevent causalities before they happen. This is called "a priori" control, control that is gained before the fact, not after something goes wrong.

There are three basic strategies for winning the war on variation.

1) A priori control during the product and process design cycle:
   - Define Six sigma tolerances on all critical product and process parameters
   - Minimize the number of parts in the product and minimize the steps that comprise the process

- Standardize the parts and processes used
- Use SPC principles and computer tools during the design and prototype phase

2) Use SPC to continually isolate, control and eliminate variation resulting from:
- People, Machines, Material, Environment

3) Suppliers must continually strive to eliminate variation in the parts and materials we purchase as follows:
- Instituting a supplier qualification program which is part based on SPC principles
- Require Process Control Plans
- Minimize the Number of Suppliers that are used
- Ensure Long Term "win-win" partnership with the suppliers"

Designing Six Sigma (6σ) into the product

Designing for Manufacture: Manufacturability as defined by Motorola Inc. (1987) *as the ability to produce identical products without waste, so that the products satisfy all customer physical and functional requirements (quality, reliability, performance, availability, and price) and also satisfy business goals.*

Translating this into statistical terms, (from the design engineering perspective), *is the ability to characterize the various product and process elements that exert an undue influence on the key product response parameters in such a manner that the critical product quality, reliability and performance characteristics display:*

a) Robustness to random and systematic variations in the central tendency (Mu = μ) and variance (Sigma squared = σ^2) of their physical elements.

b) Max. tolerances related to the "trivial many" and optimum tolerances for the "vital few".

c) Minimum complexity in terms of product and process elements count (*fx*).

d) Optimum processing and by such indices as cycle time, rolled throughput yield.

The implied objectives can be realistically achieved as follows:

a) Identify critical characteristics through such functions and activities as marketing, industrial design, R & D engineering
b) Identify the product elements that influence the critical characteristics defined in step 1
c) Define the process elements that influence the critical characteristics defined instep 2
d) Establish maximum tolerances for each product and process element defined in steps 2 & 3
e) Determine actual capability of the elements presented in steps 2 & 3
f) Assure Cp >2, Cpk >1.33

The Design Perspective

Historically, Western manufacturing has followed the "throwing over the wall" practice. Design Engineers design the product, Manufacturing Engineers build the product (and actually re-design the product for production), and Quality Engineers inspect the product. Mikel J. Harry *in The Nature of Six Sigma* says that "Design philosophy has, in general been one of establishing a design based on experience and best engineering judgment followed by the conduct of worst-case analysis. At this point, the design is assessed for producibility. If such a study yields unsatisfactory results from a manufacturing point of view, components are redefined and tolerances are constructed in some combination until satisfaction is derived.

This particular school of thought says that the quality is improved by deliberately trying to restrict the total amount of performance variation through the use of more expensive parts, "tweeking" devices, protective subsystems, and tighter tolerances all the way around. In many instances, such a philosophy forces higher parts counts that otherwise would be necessary which in turn substantially increases product complexity-all of which translates into a manufacturing system characterized by excessive defect levels, cycle time, inventory, and labor costs. The key is to design in consideration of variation- not around it."

"In more recent times, attention has turned to the Taguchi philosophy of product design. The Taguchi philosophy advocates that the product design can be made robust to natural part variations through either empirical or computer-simulated experiments, or even both. Most often, the simulated experiments are driven by some type of computer-based response engine or "performance algorithm" as it is often called."

PARTS PER MILLION CALCULATIONS

Parts per million are defined in the automobile industry as the number of defective parts per million. If you had 1000,000 parts and 5000 were defective, you would call this 5000 defects per million.

Motorola defines PPMs in a different manner. Number of assemblies within a process are identified. The number of solder joints within an assembly are enumerated. The number of possible defects within a process are listed. Opportunities are defined as the total number of opportunities for mistakes in a particular system.

- 1 Electronic System = 20 PWBs (500 solder joints each) = 10,000 solder joints
- The number of solder joints = Opportunities
- The number of defects/ # of opportunities = PPM = Defect Per million opportunities or = DPMOs = Nonconformance Per million opportunities
- Add all the defects in the assemblies that go in a unit to get Total Defects per unit = TDU
- Convert DPMOS to Sigma (σ) based on the tables

PROCESS CAPABILITY STUDIES

The *natural variation of a process,* (after special causes of variation are eliminated) is called "Process Capability". Process capability Studies are undertaken to measure the inherent variability of the process so that the performance potential can be detected under normal, in-control conditions. Control chart methods are used for measuring process capability at a 99.7 % confidence level.

The process capability can be applied to the following conditions:

1) Information to facilitate the design of the product
2) Acceptance of new or reconditioned piece of equipment
3) Scheduling of work to machine
4) Setting up the machine for a production run
5) Selection of operators
6) Determining the economic nominal around which to operate when process capability exceeds the tolerance

Cp and Cpk in industries with product specification limits

Comparisons of process capability to engineering specifications are used to assess whether a process is able to meet the requirements. These are called capability ratios. One ratio is the *Cp*, the other is called *Cpk*. Capability studies in non-electronic manufacturing sector are easy to calculate. The engineer already knows the specifications *Upper Spec. Limit* (USL), and *Lower Spec. Limit* (LSL). We know the spread of a typical process is plus and minus 3 sigma (σ). Process capability is defined as six standard deviations. It is the potential of the Process.

The Capability indices are calculated as follows:

Cp Index: Implies relationship between specification width and natural tolerance
Cp = Engineering Tolerance/ Process Spread

$$Cp = \frac{USL - LSL}{6\sigma} \quad \text{.....(1)}$$

Cpk Index: Describes in terms of the distance of the process average from the specification limits in standard deviation units. A modification of the Cp ratio is the Cpk ratio which takes into effect the centering of the process relative to the target. Assess actual process performance.

Cpk = Closest Spec/ Half Process Spread .....(2)
Cpk = X-Bar - Closest spec/ 3 Sigma .....(3)

$$Cpk = \frac{\bar{x} - \text{Closest Spec}}{3\sigma}, \quad Cpu = \frac{USL - \bar{x}}{3\sigma}, \quad Cpk = \frac{\bar{x} - LSL}{3\sigma} \quad \text{.....(4).....(5)....(6)}$$

Both ratios assume that only common cause variation are present. If special causes are present, then the information given by the ratios is not very reliable. Therefore the control Charts which supply the process average (the X-Bar) and the variation about the average (the Range Chart) must be in control. The Cp ratio which is not tied to a target value is useful in determining the process potential, while the Cpk ratio, which is tied to a target value, is used to assess actual process performance. When calculating capability ratios, the amount of data collected must be taken into account, even if the process is in control. The more data that is available the more reliable the Cp and Cpk ratios will be. Process capability is measured by the process performance ratio Cp and Cpk. Many companies use Cp and Cpk of 1.33 as a target.

- Cpk values by themselves do not mean much, It is how much they improve
- Cpk < 1.00 is very poor
- Cpk = 1.00 to 1.32 is fair
- Cpk > 1.33 excellent
- Cpk is not a substitute for Cp. They work together and compliment each other

Absolute Cp and Cpk are not very important because their values depend upon spec. limits. Spec limits are arbitrary anyway. What is important is Progress of Process improvement.

Capability Studies (Cp and Cpk) in electronic manufacturing

In Attribute data we do not have Upper or Lower Spec Limits. How do we calculate Capability Indices in the electronic industry or in areas where gathering variable data is too costly to collect? We Calculate PPM, Calculate z, Plug into the formulae, Cp = (z + 1.5)/3, Cpk = z/3, (z is explained within the next few pages).

TABLE 8. Sample Process control plan for variable/attribute data

Component/Process	Characteristic	Inspection Equipment	Sample Size Frequency	Analysis Target	CP Index

For Attribute Data, the process capability is indicated by the average performance (example p, np, c, u) as long as the process is in statistical control. For example, if the process yields 2% nonconforming product, use the 2% process average as a target. The goal is to continually strive to lower the current process average through systemic improvement.

DEFINING THE STANDARD NORMAL CURVE

So How do I calculate this "z" number? Very simply look under Standard Normal Distribution Tables.

- Normal curve can be calculated by calculus
  - Integration of functions between two points
  - Integration of one particular Distribution is called the Standard Normal Distribution. SND is shown as "z" displayed under z-tables (SQC by Grant and Leavenworth)
- Standard Normal curve: Important use of curve is:
  - Easy to calculate area under the curve
  - Total area under the curve = Total relative frequency for distribution = 1
  - Curve is symmetrical
  - Area under either side is = .5
- The Standard Normal Distribution Curve is the Normal Distribution Curve with conditions:
  - Zero Mean (Mu = $\mu = 0$)
  - UNIT Standard Deviation = Sigma = $\sigma = 1$)

$$f(x) = \frac{1}{\sqrt{2\Pi}^{\frac{x^2}{2}}} \quad \text{.....(7)}$$

This is how you calculate area under the z curve

CALCULATING PPM FROM Z TABLES and Cp FROM PPM

- **Question: If Cpu = 1.15 and Cpl = 1.08, Find the value of PPM = ?**
  - **Step 1**
    - » Zu = 3(Cpu) = 3 (1.15) = 3.45 .....(8)
    - » Zl = 3(Cpl) = 3(1.08) = 3.24 .....(9)
  - **Step 2**
  - Locate fraction defective values for Zu and Zl from tables (*At end of any Statistics book*)
    - » For Zu = 3.45, find 3.4 in the leftmost column of z table
    - » and .005 in the uppermost column at intersection of 3.4 and .05 find value of
    - » 2.804E-.04

Similarly Zl = 3.24 or 5.977E-04

- **Step 3**
  - » Convert values from table to PPM
  - » 2.804E-04 = 0.0002804
  - » 5.977E-04 = 0.0005977
- To convert to a ppm level, the fraction defective value should be multiplied by 1,000, 000
- Therefore:
  - » Cpu = 0.0002804 (1,000,000) = 280.4 ppm
  - » Cpl = 0.0005977 (1,000,000) = 597.7 ppm
- **Step 4**
- Add ppm obtained in Step 3 for Cpu and Cpl. Therefore, the total ppm quality level is: 280.4 ppm + 597.7 ppm = 878.1 ppm

Calculating Capability Ratios from the PPM numbers

PPM can be calculated by counting the # of opportunities (e.g.: # of solder joints on a board). For a product, the # of assemblies have to be taken into account.

If you have the PPM values from data use the following formulae to calculate Cp and Cpk for attribute data. Plug the above values of PPM to reverse check your answer.

$$Cp=\frac{Z+1.5}{3\sigma}, \quad Cp=\frac{Z}{3} \qquad \text{.....(9)....(10)}$$

- **Question: If PPM = 300, Find Cp and Cpk?**

Out of 10,000 devices we have 3 rejections. The reject rate is: 3/10,000 = .0003 or 300 ppm
300 ppm equals 3.44 sigma (σ). Cp = 3.44 + 1.5 = 4.94/3 = 1.65

SAMPLING PLANS AND SAMPLE SIZE

Sample sizes are established on the particular process and the volume of production. Once the process has been brought under control and the process is capable, then we can begin eliminating inspection. At this juncture, we begin looking at "some" parts during a shift. Appropriate sampling plans can be chosen using Mil-Std-105 procedures. The sample size has a direct bearing on the control limit so it is extremely important that we adhere to a reasonable sample size.

PRE-CONTROL CHARTS

The charts used for the purpose of eliminating inspection are called "Pre-Control-Charts". The Pre-Control-Charts are really Post-Control Charts, and are sometimes called "Rainbow charts" because of the colors. The Pre-Control-Charts are divided into Green Yellow and Red Zones. If the sample inspected falls within the green zones, we continue with the process. If the samples fall within the red or yellow zones, then we take appropriate corrective actions.

Pre-Control techniques follow rules as explained below. These should be modified:

1) *Set up:* Sample 5 pieces in a row. OK to run 5 in a row when 5 are inside the target

2) *Running:* Sample 2 pieces from the first lot and or periodically (Once process has shown itself to be capable)

If first piece is within target, run the lot. If the first piece is not in target, check the second piece.

If both pieces are out of target, go back to setup rule 1.

THE FUTURE OF SPC

SPC is not a quality fad. It is here to stay. A list of American corporations using SPC is a list of successful American corporations. Many corporations and service industries are using SPC to continuously monitor and improve themselves. As more and more companies realize the use of statistical techniques, the use of SPC will grow. Metrics, sensors, yield rates are all data gathering and data analysis techniques that have been adapted by American corporations.

DESIGN OF EXPERIMENTS AND TAGUCHI METHODS

SPC is more of a process monitoring tool. As we move towards optimizing particular products and machines, we need advanced statistical techniques to optimize the output. Design of Experiments are set up on particular hardware to improve the system. DOE provides a systematic way to design an efficient experiment, collect the data and analyze it.

Factors: The independent variables (inputs) that are controlled in the experiment are called factors.
Factor Levels: The settings of the factors in the experiment are called factor levels.
Response: The dependent variable, that is the outcome of the experiment is called response.

The goal of the experiment is to determine the relationship between the factors and the response.

Once experiment has been run, three general analysis may be done.

1) Analysis of Variance (ANOVA). Perform Regression Analysis
2) Interprets the results visually on a variety of graphs
3) Analyzes the differences between the outcomes of the experiment (*observed responses*) and responses predicted by the first type of analysis (*predicted responses*). The difference is called *residuals.*

CONCLUSION

Motorola and other world class companies have set the tone for quality improvement in the electronics industry. Most computer statistical packages sold in the United States deal with Variable data. Those that do deal with Attribute data do not go into the depth that they need to. The buyer of computer software needs to be aware that additional computation will be necessary.

The use of SPC in the Electronics Industry is essential and the usage can add substantial profits to the bottom line. As the use of SPC spread, newer statistical techniques will evolve. It is imperative that we keep up with the latest developments.

BIBLIOGRAPHY

1. *Statistical Quality Control* by Eugene Grant and Leavenworth
2. *AT&T Statistical Quality Control Handbook* published by ASQC
3. *Process Improvement in the Electronic Industry* by Yefim Fasser and Donald Brettner
4. *Engineering Statistics and Quality Control* by I. Burr
5. *Economic Control of Quality of Manufactured Products* by W.A. Shewhart
6. *The Nature of Six Sigma Quality* by Mikel J. Harry
7. *Six Sigma Producibility Analysis and Process Characterization* by J. Ronald Lawson and Mikel J. Harry

APPENDIX A

The following chart assumes plus minus 1.5 sigma (1.5 σ)shift

"SIGMA"(σ)	PPM	Cp	Cpk
1.5	500,000	.50	.00
1.6	460,172	.53	.03
1.7	420,740	.57	.07
1.8	382,089	.60	.10
1.9	344,578	.63	.13
2.0	308,538	.67	.17
2.1	274,253	.70	.20
2.2	241,964	.73	.23
2.3	211,855	.77	.27
2.4	184,060	.80	.30
2.5	158,655	.83	.33
2.6	135,666	.87	.37
2.7	115,070	.90	.40
2.8	96,801	.93	.43
2.9	807,57	.97	.47
3.0	66,807	1.00	.50
3.1	547,99	1.03	.53
3.2	44,565	1.07	.57
3.3	35930	1.10	.60
3.4	28717	1.13	.63
3.5	22750	1.17	.67
3.6	17864	1.20	.70
3.7	13903	1.23	.73
3.8	10724	1.27	.77
3.9	8198	1.30	.80
4.0	6210	1.33	.83
4.1	4661	1.37	.87
4.2	3467	1.40	.90
4.3	2555	1.43	.93
4.4	1866	1.47	.97
4.5	1350	1.50	1.00
4.6	967.7	1.53	1.03
4.7	687.2	1.57	1.07
4.8	483.5	1.60	1.10
4.9	337.0	1.63	1.13
5.0	232.7	1.67	1.17
5.1	159.2	1.70	1.20
5.2	107.8	1.73	1.23
5.3	72.4	1.77	1.27
5.4	48.1	1.80	1.30
5.5	31.7	1.83	1.33
5.6	20.7	1.87	1.37
5.7	13.4	1.90	1.40
5.8	8.6	1.93	1.43
5.9	5.4	1.97	1.47
6.0	3.4	2.00	1.50

APPENDIX B
Which defects to monitor?

Mil-Std-2000 (no change) gives us an excellent starting point to figure out the kinds of defects that we need to monitor in Electronic Manufacturing. The listing includes Reworkable *Defects* and Non-Reworkable Defects called *Process Indicators*: Mil-Std-2000A has a shorter defect list. Many engineers are using the Mil-Std-2000 listing. This list has been embellished and is reproduced here.

SOLDER DEFECTS
(Defects that need to be reworked)

Lifted/Tilted Parts
Warping
Solder on connector
Solder Balls on Board
No Solder
Bridging
Cold Solder
Fractured
Disturbed
Insufficient Solder
Excessive Solder (Lead not Discernible)
Splatters
Pinholes, Voids
Solder Peaks
Missing Parts
Excess Solder in the Bend
Other

PROCESS INDICATORS
(Defects monitored, not reworked)

Component not resting on feet pads or projections
Component not mounted perpendicularly
Component abrasion with another component
Lack of solder coverage on lead ends
Excessive solder (Lead is discernible)
Component is not centered
Pits, pinholes, voids (bottom of pit is visible)
Unfilled plated through hole
Measling or crazing
Other

In addition to the above, for SMT the following defects should be monitored :

SMT DEFECTS
(Defects that need to be reworked)

Wrong Component Placement
Wrong Orientation
Missing Component
Component Mis-Alignment
Damaged Component
Charring of Component
Cracked Joints
Voids
Disturbed Joints
Drawbridging
Webbing
Tombstoning
Solder Skip
Spatter
Crystallized Solder
Dispersion
Other

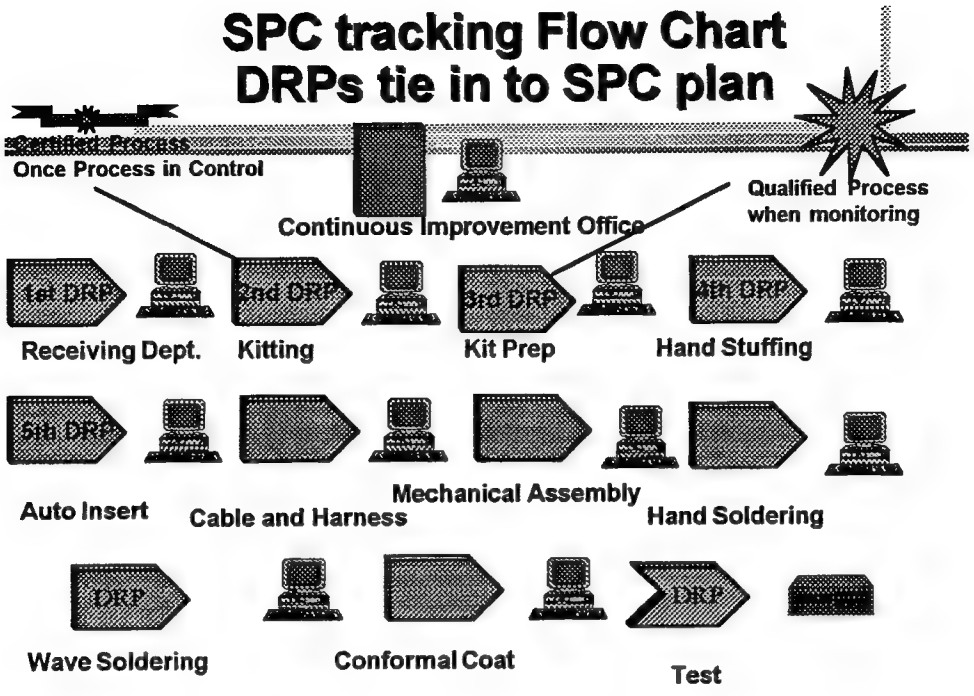
PROCESS INDICATORS
(Defects monitored, but not reworked)

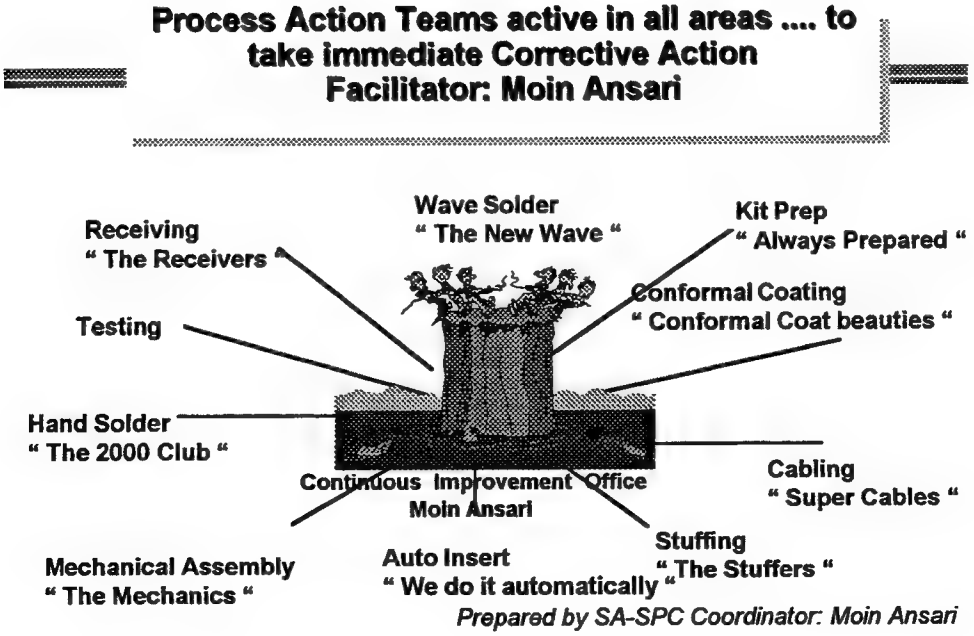
Component not resting on feet pads or projections
Component not mounted perpendicularly
Component abrasion with another component
Lack of solder coverage on lead ends
Excessive solder (Lead is discernible)
Component is not centered
Pits, pinholes, voids (bottom of pit is visible)

Measling or crazing
Other

Similar defects have been developed for MCM and BGAs. Some companies may want to relax their Reworkable defect criteria if they want to reduce assembly costs. Most companies have found out that relaxing these "inspection criteria" adds cost in the long run in terms of customer complaints, customer returns, and test failures.

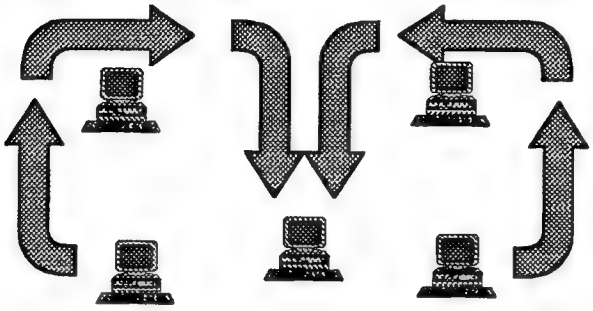
I


SPC tracking Flow Chart
DRPs tie in to SPC plan
Certified Process
Once Process in Control
Continuous Improvement Office
Qualified Process
when monitoring
1st DRP
2nd DRP
3rd DRP
4th DRP
Receiving Dept.
Kitting
Kit Prep
Hand Stuffing
5th DRP
Auto Insert
Cable and Harness
Mechanical Assembly
Hand Soldering
DRP
DRP
Wave Soldering
Conformal Coat
Test

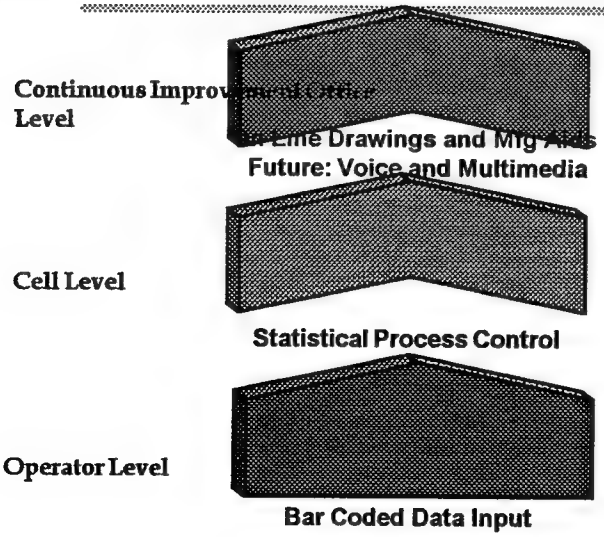

Process Action Teams active in all areas .... to
take immediate Corrective Action
Facilitator: Moin Ansari
Wave Solder
" The New Wave "
Receiving
" The Receivers "
Kit Prep
" Always Prepared "
Conformal Coating
" Conformal Coat beauties "
Testing
Hand Solder
" The 2000 Club "
Continuous Improvement Office
Moin Ansari
Cabling
" Super Cables "
Stuffing
" The Stuffers "
Auto Insert
" We do it automatically "
Mechanical Assembly
" The Mechanics "
Prepared by SA-SPC Coordinator: Moin Ansari

II

Data Monitoring Equipment in Focused Factory Cells

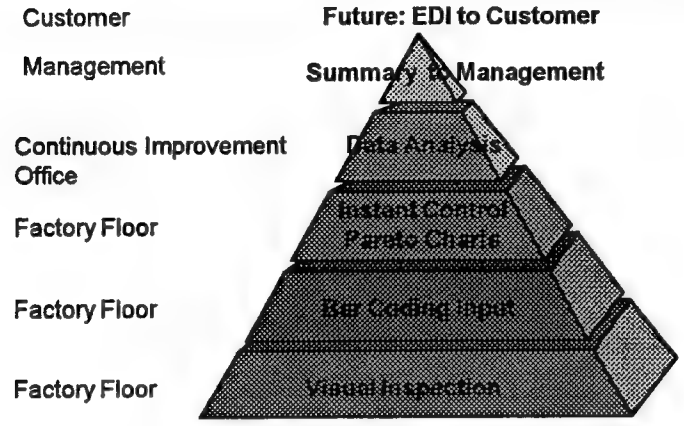


SPC Data Analysis



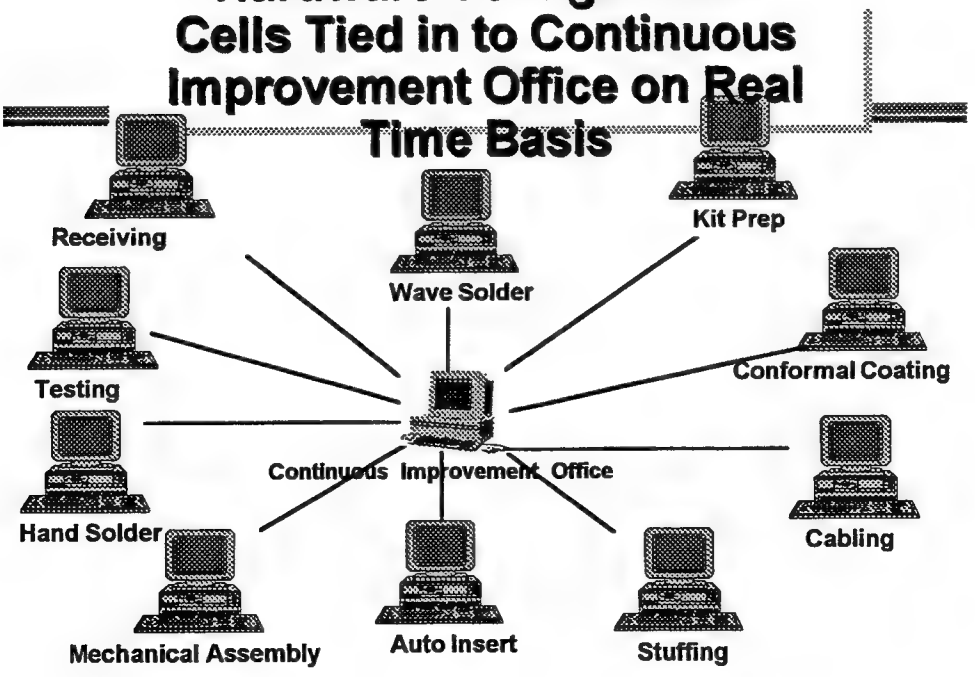
III

Data Flow Pyramid

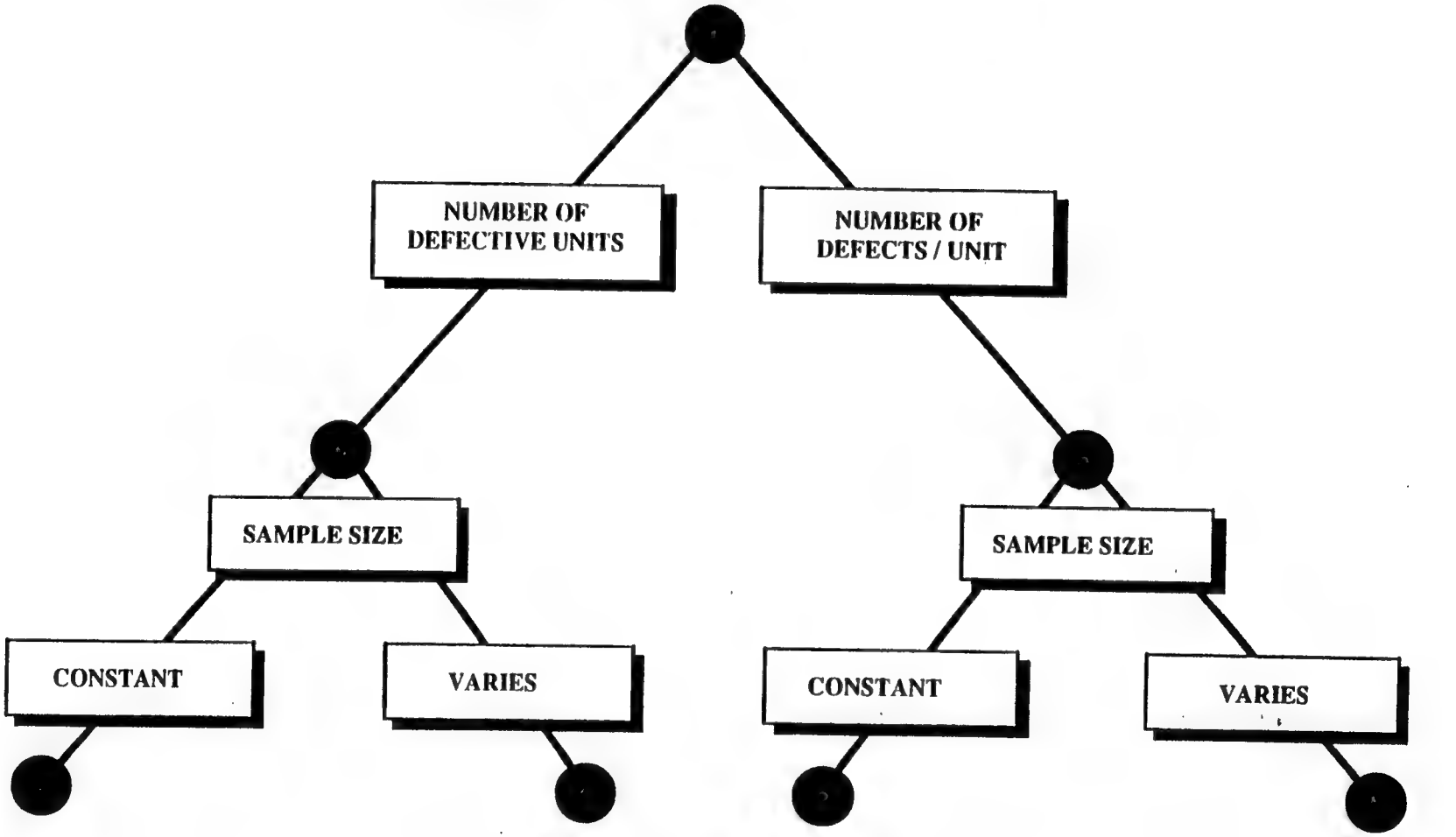


Prepared by SA-SPC Coordinator: Moin Ansari

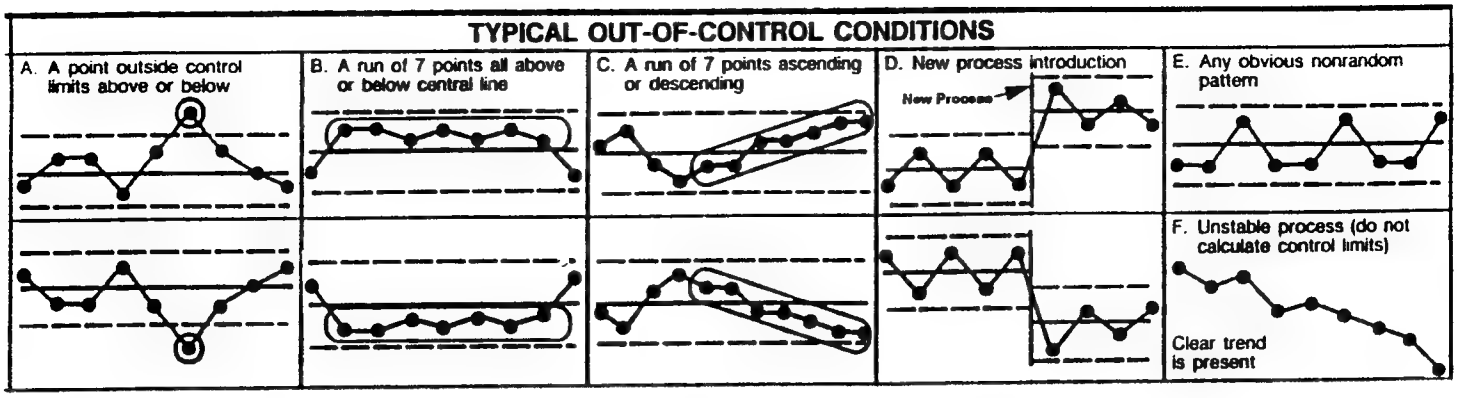
Hardware Configuration Cells Tied in to Continuous Improvement Office on Real Time Basis

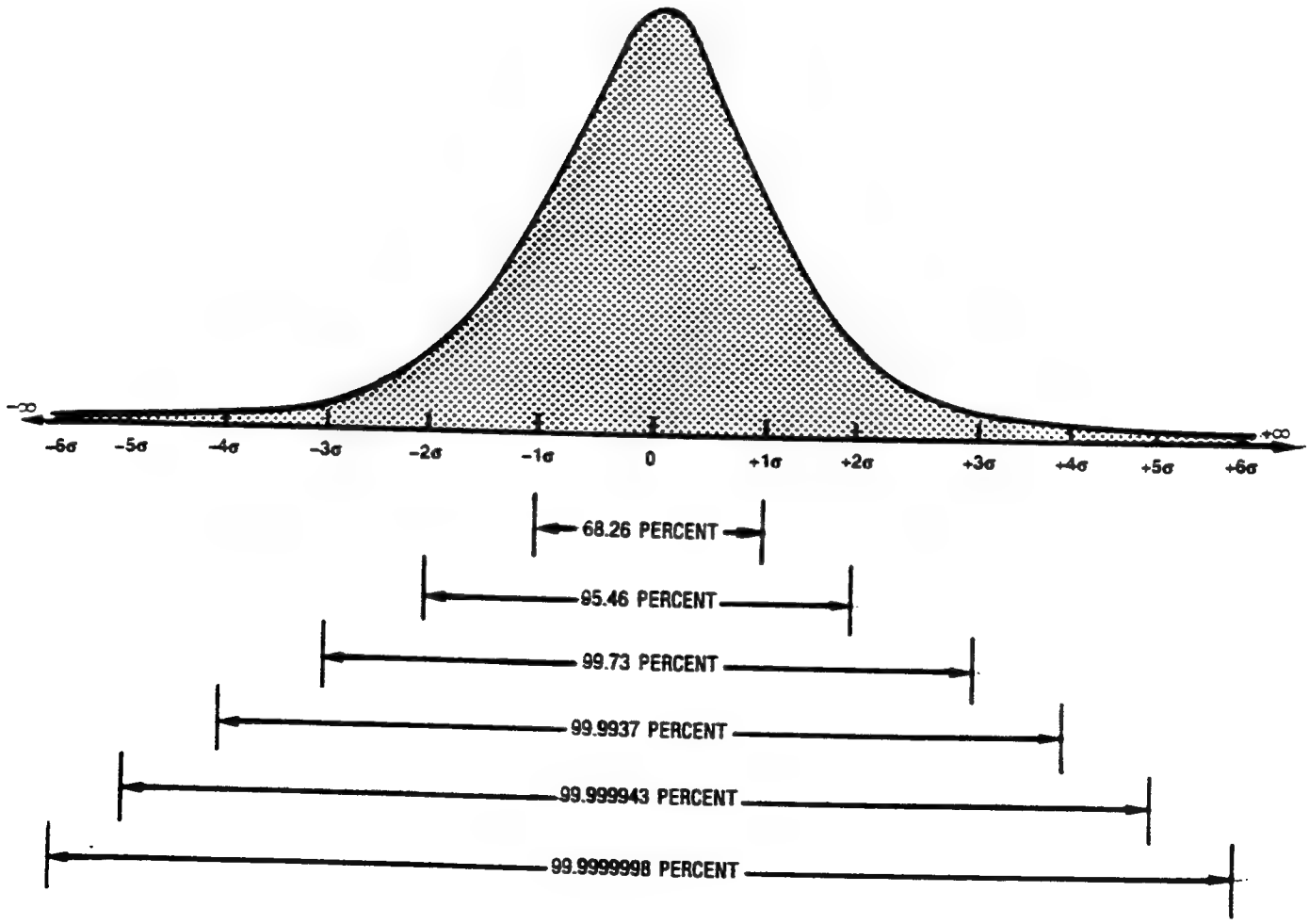


ATTRIBUTE CHARTS



Use this type of chart !





Typical Areas Under the Normal Curve

Moin Ansari, B.S.I.E., B.A., M.B.A.A., is a certified Manufacturing and Marine Engineer and President of Irvine Engineering & Consulting (IEC) with over 15 years of engineering experience. He manages continuous improvement programs at Scientific-Atlanta (S-A), Inc., San Diego, California. He is responsible for statistical process control (SPC), high reliability soldering, paperless information systems, ISO-9000, and training. As part of the S-A center of excellence, he implemented a state-of-the-art PC-LAN based SPC defect reduction program. He is a member of the corporate Operations and Quality Councils, planning long-term strategic initiatives for the entire company. He is the corporate SPC facilitator charged with proliferating SPC in all the divisions.

He has authored a book, *World Class Manufacturing*, and has written articles on quality and manufacturing. He teaches World Class and Computer Systems in Manufacturing, Soldering for the 21st Century, and ISO-9000. He is a consultant on a steering committee for an NIST/Department of Commerce research project that deals with improving electronics manufacturing systems through statistical software.

His master's thesis project was "The Effectiveness of World Class Manufacturing on Companies in the U.S." A specialist in the Toyota Production System and Japanese "Kaizan" techniques, he holds seminars and speaks at international forums and universities, including UCLA, QAU, and GIK-IST.

In February 1994 he received the Outstanding Employee "WIN" award at S-A. As a result of world-class manufacturing efforts, his SPS Division was declared a Center of Manufacturing Excellence for all of Scientific-Atlanta.

Address: Irvine Engineering & Consulting
194 Streamwood
Irvine, CA 92720-1933

CONFORMAL COATING PROCESS OPTIONS

By Richard Quade and Roger Olson
Specialty Coating Systems, Inc.
Indianapolis, Indiana

ABSTRACT

Printed circuits and circuit assemblies are commonly protected against environmental and electrical threats by a conformal coating. Such coatings may also be used to alter surface characteristics or to dampen mechanical vibration. Electronic manufacturers must choose between a variety of coating materials and application processes to achieve the desired protective effect with efficiency and economy.

Recent environmental regulations have had a significant impact on both conformal coating materials and methods. Manufacturers have responded by developing non-solvent coatings and environmentally friendly application and curing systems. Today users may select from a variety of coating materials with varying properties and characteristics, depending on the requirements of their applications. Coating system efficiencies are being improved in response to strict waste disposal regulations and the cost of sophisticated new materials.

A number of conformal coating process alternatives may be considered, including brush, dip, spray, selective spray, wave, and vacuum deposition application methods. Each of these application techniques is characterized by unique benefits and limitations, which are reviewed in this paper to assist production engineers in selecting the optimum coating process.

BACKGROUND

Conformal coating is often used to protect printed circuits and circuit assemblies against environmental threats that include moisture, chemicals and damaging vapors. Coatings also prevent disruption and circuit damage caused by inadvertent electrical shorting, or conductive paths between conductors that can develop as a result of condensation or contamination. Conformal coatings can also alter surface characteristics and physically stabilize components.

Advancement of conformal coating technology has been fostered primarily by the requirements of military systems over the past several decades (per MIL-I-46058C, Army Regulation 70-71, NAV. INST. 3400.2, USAF-80-30). More recently, sophisticated coating materials and techniques have been adopted for industrial, automotive, medical and commercial electronic products as well, to the overall benefit of both military and commercial applications.

Changing environmental regulations are having a significant impact on both coating materials and processes, resulting in a strong demand for solvent-free coating processes. Manufacturers are responding with development of materials such as 100% solids coatings cured by ultraviolet, thermal or moisture processes rather than through solvent evaporation. Non-solvent coating materials are now available with a range of properties and characteristics in formulations that include urethanes, silicones, epoxies, acrylics and poly-para-xylylene (parylene).

Conformal coating system efficiencies are being improved in response the cost of sophisticated new coatings as well as waste disposal regulations. Several conformal coating process alternatives may be considered, including brush, dip, spray, selective spray, wave and vacuum deposition application methods. Each coating technique is characterized by distinct benefits and limitations. Options are presented here to help production engineers identify the optimum coating method for given manufacturing applications.

Boards must be completely clean to prevent flux residues or other ionic contaminants from being trapped under the coating. Such contaminants can result in degraded circuit performance or failure. Regardless of the appliction method selected, a conformal coating must be without pinholes or gaps in coverage. Incomplete coverage can result in migration of under the coating over time, resulting in corrosion and circuit malfunctions.

Coating parameters to be considered in selection of a coating process include circuit preparation, coating adhesion promotion, material transfer efficiency, coating thickness control, prevention of bridging between components, coating removal for circuit repair, thermal expansion considerations, and environmental performance requirements. The matrix at Figure 1 shows the spectrum of coating process characteristics to be considered.

COATING PROCESSES

FEATURES	Brush	Dip	Spray	Selective Coating	Wave	Vacuum Depos.
Adhesion Promotion	never	never	rarely	never	no	usually
Transfer Efficiency	modest	poor	poor	good	good	modest
Thickness Control	poor	poor	good	modest	good	excellent
Thickness Linearity	poor	poor	modest	modest	good	excellent
Bridging Performance	bridging	bridging	bridging	bridging	bridging	non-bridging
Masking	required	required	required	none	required	required
Applicability	2-side	2-side	1-side*	1-side*	1-side	2-side
Edge/Point Coverage	poor	poor	poor	poor	poor	excellent
Voids/Pinholes	yes	yes	yes	yes	yes	no
Envir. Performance	poor	good	modest	modest	good	excellent

**Special equipment design can accomodatetwo-sided coating applications.*

Figure 1 - Conformal Coating Process Characteristics.

CONFORMAL COATING METHODS

BRUSH

Perhaps the simplest and least sophisticated means for applying protective coatings is by hand brushing. This process is simple, requires little investment, and depending on the coating required, may be suitable for low volume work, with either single or double-side coverage. Brush application (Figure 2) depends on operator attention for completeness of coverage and thickness uniformity of thickness. Manual brush application of conformal coatings is generally restricted to situations where the coating is only marginally important. Materials used with this method are generally "air dryable" solvent-borne or moisture cure materials.

DIP

Where overall coverage is required, dip coating (Fiigure 3) may be appropriate. Conveyorized dip systems typically transport boards in the vertical position on wire hooks or quick-disconnect fasteners for immersion in a coating reservoir, after which excess coating is allowed to drip off before UV heat curing. Contacts, connectors, test points, switches and other PCB areas must be masked before dip coating, and then unmasked after curing is complete.

Dip coat coverage tends to be thicker at the bottom portion of boards due to sagging, and average coating thickness is likely to exceed actual protection requirements. A dip coating system almost always requires manual mounting and removal of circuits. This coating method is appropriate for applications that require complete board coverage, and/or on circuit boards with relatively simple masking requirements.

SPRAY

This method of coating application (Figure 4) is suited to conveyor handling in an in-line manufacturing environment, with either fixed or articulated spray heads. The simplest spray systems use one or more fixed spray heads along a conveyor that are activated by passing boards. While capable of good coverage and excellent uniformity with less material consumption than dip coating, spray coating may not be capable of reaching beneath closely spaced circuit board components.

Two-side circuit spraying can be accomplished using complex conveying and handling mechanisms to invert boards during the spray cycle, but most systems coat one side at a time. Sprayed circuits must be masked and unmasked to protect selected areas; however, masking does not need to be liquid tight as is the case with dip coating. Rubber boots, tape and cardboard cutouts serve as temporary maskants.

Overspray is typically captured by a paper conveyor liner, which must be disposed of in an approved manner. Spray coating is most commonly used for high volume applications that require more masking than would be tolerable in a dip coating situation.

Selective Spray - More sophisticated robotic systems are available that use airless spray guns mounted on robot arms to deliver coating to selected areas on a PCB (Figure 5). Spray head movement cycles are pre-programmed to reach every area on mechanically complex substrates. These machines work well with solvent-borne coatings but tend to deposit excessive material when used in conjunction with newer 100% solids, UV or thermally cured coatings, resulting in unwanted coating thickness. Such systems also tend to be slow, making them unsuitable for high volume coating work.

Select Jet Spray - A new selective spray circuit coating method recently developed by Specialty Coating Systems uses a process that is analogous to ink jet printing (Figure 6). This new design has multiple coating emitters arranged in a matrix, and these emitters can be cycled on and off individually under computer control to achieve selective coverage. Selective coating eliminates the labor and cost of masking and unmasking, and is capable of achieving pinhole-free integrity with substantially less coating consumption than standard spray or selective spray coating techniques.

This new process also eliminates overspray and the resulting disposal requirements. Selective spray coating is a single-side process accomplished on the underside of circuit assemblies, although systems can be designed to flip boards for a second coating pass. The line-of-sight selective coating process is not capable of reaching under components.

WAVE

In this process, a wave of coating - similar to molten solder in a wave soldering system - is created by pumping the liquid material through an aperture (Figure 7). Inverted circuits are conveyed across this wave. The coating material may be heated to adjust its viscosity and improve surface wetting. Precise adjustment of the pumped wave height and shape are difficult, and production speeds may be limited with this process.

Some wave coating systems use a brush to strip off and recover excess coating from boards after contact with the wave. Masking is required, and wave coating is a single-side process that can only be used for the non-component side of a printed circuit board. Therefore wave coating is appropriate for applications that require only bottom side coverage, or in combination with a spray or selective spray system in order to coat both sides of the circuit without inverting boards.

MEGASONIC WAVE COATING

A Specialty Coating Systems adaptation of conventional wave coating, this process creates a stable coating wave by means of megasonic activation (Figure 8). A piezo-electric transducer immersed in a coating bath directs radio frequency energy at the coating surface by means of a parabolic emitter.

This RF energy creates a much more consistent, controllable wave of coating above the surface than is possible with a pumped wave, increases coating temperature and viscosity, and results in a molecular scrubbing action that penetrates the substrate boundary layer for improved liquid contact.

Megasonic Wave Coating augments coverage and reduces coating consumption compared to conventional wave coating. As with conventional wave coating, the Megasonic process is most appropriate for bottom-side coating of circuit assemblies. Both wave methods are limited to assemblies with component and lead heights of 3/16 inch or less below the board.

MENISCUS COATING

Yet another proprietary Specialty Coating Systems design, the meniscus coating process (Figure 9), uses a permeable tube through which coating is pumped to create a continuous fountain. Inverted assemblies are passed through the fountain, and as a moving substrate intersects with the coating liquid, menisci are formed at the leading and trailing edges.

Meniscus coating is capable of far greater accuracy and linear coverage than spin coating with essentially no material waste. The primary use for this process is application of specialty materials to essentially flat substrates such as glass or metalized glass display panels or silicon wafers. Not intended for traditional circuit board work, the meniscus process is primarily a replacement for spin coating. It is capable of laying down coatings in thicknesses from 0.1 micron to approximately 10 microns.

Meniscus coating achieves ±2% thickness accuracy regardless of the microplanarity of the surface, and gives essentially linear coverage across a substrate (unlike spin coating, which uses centrifugal force to distribute coating material).

VACUUM DEPOSITION

This dry, solvent-free coating process (Figure 10) is designed to coat circuit board assemblies and other substrates with a thin, inert and highly conformal polymer film known as parylene. The raw material for the process is di-para-xylylene dimer, a dry powder.

Objects to be vacuum coated with parylene are cleaned, masked, and in some cases treated with an adhesion promoting agent. They are then fixtured in a vacuum chamber where a gaseous monomer polymerizes on all surfaces to create a pinhole-free, transparent and very thin film. Parylene is highly inert, has high dielectric properties, and matches or exceeds the coating parameters of liquid materials, at one-tenth or less the thickness.

There is no cure phase in this process, no emissions and no disposal issues. Gas phase deposition ensures that coating thickness is equivalent on all surfaces, including planar areas, crevices, edges and corners. The polymerizing gas does not exhibit liquid properties such as meniscus, bridging between adjacent components or pooling in low areas. Because of the nature of the deposition process, parylene does not create mechanical stress during deposition, and does not create stress on underlying components during subsequent thermal cycles.

The vacuum deposition coating process is most appropriate where coating effectiveness must be very high, where it is important to minimize coating mass because of thermal coefficient of expansion or other considerations, and where excellent solvent or moisture resistance is required.

SUMMARY

There are many combinations of coating material, process and equipment to be considered in selecting the optimum conformal coating process for a given circuit assembly. The optimum method will be determined by production volume, performance requirements, circuit complexity and related factors. Equipment suppliers may be helpful in assessing requirements and implementing a standard or adapted coating process.

ILLUSTRATIONS

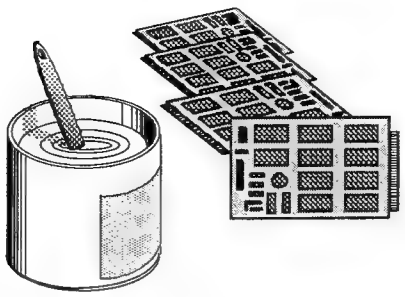


FIGURE 2 - The simplest means of applying a conformal is manually, using a brush.

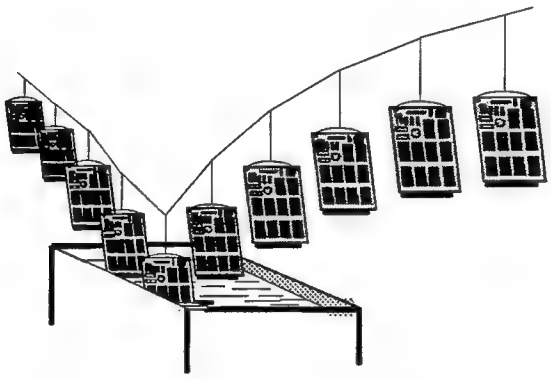


FIGURE 3 - A Dip Coating system immerses assemblies in a liquid bath.

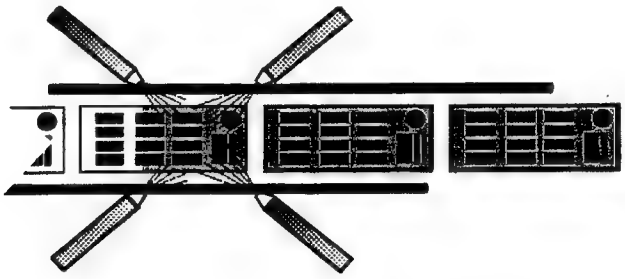


FIGURE 4 - A fixed spray coating system uses fixed spray heads adjusted to cycle on as a board is conveyed past the coating station.

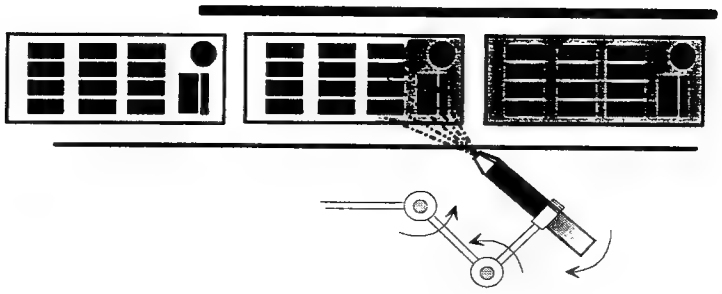


FIGURE 5 - A robotic spray coating system is more effective in coating complex assemblies than a conventional fixed head system. The system is programmed to suit the needs of individual circuits.

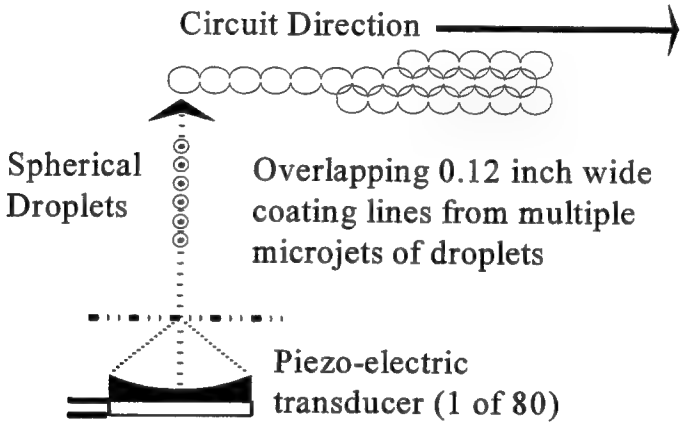


FIGURE 6 - A pulse jet selective coating system requires no board masking.

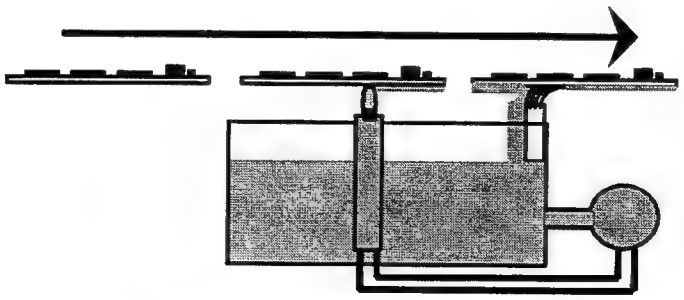


FIGURE 7 - A conventional wave coating system uses a mechanical pump to create the surface wave.

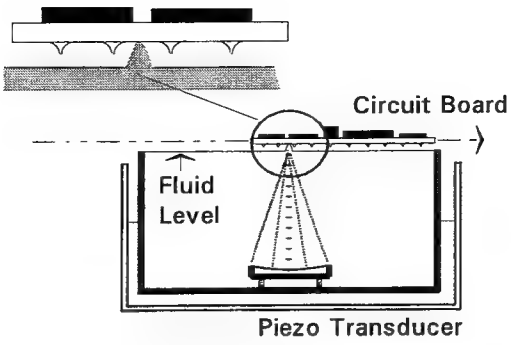


FIGURE 8 - A Megasonically activated wave coating system is activated by means of a transducer submerged in the coating material.

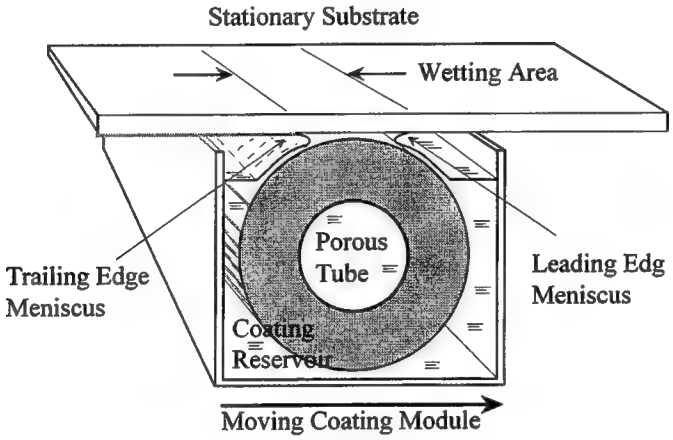


FIGURE 9 - The Cavex meniscus coating system is intended primarily for use with flat substrates such as electo-optical displays.

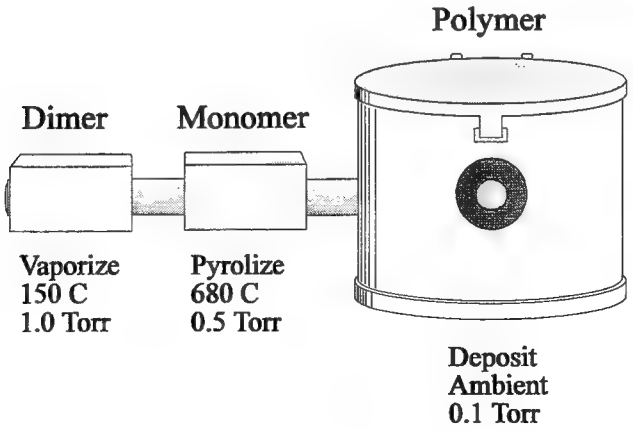


FIGURE 10 - Parylene coating is applied in a vacuum chamber at ambient temperature.

Richard Quade is Marketing Manager for Specialty Coating Systems with 7 years' experience in conformal coatings.

He has a bachelor of science degree in mechanical engineering from Case Western Reserve University, Cleveland, Ohio, and a master's in business administration from Indiana University.

Address: Specialty Coating Systems, Inc.
5707 W. Minnesota Street
Indianapolis, IN 46241

Roger Olson is Director of Technology and New Business for Specialty Coating Systems, Inc., a subsidiary of Alpha Metals, Inc.

He has been involved in the conformal coating industry for 23 years and is the author of numerous articles and publications.

He has a degree in electrical engineering from the Milwaukee School of Engineering.

Address: Specialty Coating Systems, Inc.
5707 W. Minnesota Street
Indianapolis, IN 46241

"SMT GULL-WINGS ... SOLDERABILITY ISSUES"

by

Tom Clifford
Process Specialist
Lockheed Missiles and Space
Sunnyvale, Ca.

Abstract

This paper discusses solderability issues associated with gull-wing SMT components. After the leads are formed and trimmed, the exposed base metal begins to oxidize, if unprotected, and to become non-wettable in subsequent soldering processes. This can cause solder joints of uncertain reliability. Management of this condition includes tinning by the supplier, inert storage, "just-in-time" or "first-in-first-out" scheduling, early detection, and correcting it by aggressive pre-tinning methods. This paper discusses detection (in-coming tests) and correction (pre-tinning to re-establish solderability), using a method which also appears to eliminate the bridging that often accompanies tinning of very-fine-pitch gull-wing leads.

SOLDERABILITY

SMT has come of age. Unfortunately, aging does not help the solderability of the trimmed toe-ends of gull-wing flat-packs. Oxidation develops over time. Subsequent solder processes, typically solder paste with RMA flux in aerospace applications, followed by in-line convection reflow, are often not aggressive enough to promote complete wetting of the toe. The fillet does not extend up the toe, leaving a fillet configuration that is not optimum for reliability. Figure 1 shows a typical non-wetted toe solder joint, as well as cross-section of such a joint. Recognition of this situation has triggered several activities in our labs. These include:

* Development of screening tests to detect non-wettable toe ends.
* Work with suppliers to ensure receipt of properly pre-tinned components.
* Scheduling internal form-trim, procurement and production operations in a JIT / FIFO mode to minimize elapsed time on freshly cut toe-ends.
* Nitrogen-blanket storage of exposed-toe-end components.
* Development of tinning methods to salvage components with these oxidized, non-wettable toe-ends.

TEST METHOD

Typically, incoming component verification tests identify non-tinned trimmed toes by their trim-tool scrape marks and reddish color (copper alloy lead material) or rough satin appearance (Kovar or similar alloy). At this point, it is usually not possible to determine visually whether it will be wettable. To detect a non-wettable condition to prevent later bad solder joints, incoming parts can be given a "dip-and-look" test. The

test conditions include a RMA flux dip, 2 seconds dwell in 500 F Sn63 solder, ~total transit time, examined at ~20-30X. Figure 2 shows a typical non-wetted "bad" toe-end, as well as a typical wetted "good" toe end. This method can reliably distinguish between good, bad, and medium. Finer resolution can probably be obtained from repeated samplings and careful inspection, but this has not been found necessary. Correlation between these three categories of toe-end wettability with solder-joint fillet configuration (assembled by standard process: 6 mil RMA 325-mesh paste, N2 convection reflow) has been repeatedly demonstrated. Wettable toe-ends (by this test) make good toe solder-joint fillets. Bad toe-ends make bad toe fillets. Corrected (pre-tinned) leads, using the methods described below, also have been shown to yield good solder-joint fillet configuration.

PRE-TINNING METHOD

When these problematic components are detected, it is necessary to salvage (pre-tin) the leads to ensure acceptable solder joints after assembly. The standard tinning process (up to two dips after RMA flux, 2-3 seconds immersion each, in 500 F Sn 63 solder) will not suffice for heavily oxidized toe-ends. A process has been developed that will effectively solder-coat these components, which will yield proper joints at assembly. It is based on a hot-nitrogen-knife with optional chemical pre-treatment. The solder is typically held at 485 degrees F. The gas flow is directed across the top of the solder pot. The hot nitrogen gas flow is obtained using a standard commercial hot-gas system (the type typically used for manual solder touchup), set to deliver a high-velocity gas stream at a temperature of ~210 C measured at the nozzle exit. The nozzle is a 3" wide by 1/4" deep coathanger or fan shape. The exit is mounted ~1/4" off the surface, ~ 20 degrees down, set so the gas flow velocity ripples the surface of the molten solder without displacing it. The part is held with the edge parallel with the fan exit, with the leads at a 45 degree angle. Figure 3 is a sketch of the set-up. After flux dip (normally RMA, but options are discussed below), the component lead is lowered through the knife, held in the solder for ~3 seconds, then slowly withdrawn again through the knife. During withdrawal it is possible to observe the solder bridges and icicles being blown off the leads. The solder pot temperature is held low to minimize thermal damage inside the package. The few seconds of added thermal exposure caused by the hot nitrogen flow on the leads is felt to be an insignificant additional thermal factor, and may in fact be important to the method's success. Figure 4 shows a properly wetted toe-end fillet as well as a cross-section of such a fillet.

Particularly stubborn cases of heavily-oxidized non-wettable toe-ends require chemical pretreatment. This ranges from use of the more aggresive OA flux instead of RMA flux, to a 2-16 hour presoak in room-temperature or 60 degree C concentrated citric or phosphoric acid. The hot-gas knife effect is essential in this case: these optional pre-treatments cause a striking tendency to bridge.

The processes of detection and special pre-tinning are being fine-tuned in our labs. Prevention, at the source by suppliers and lead-formers, as well as nitrogen blanket storage of vulnerable components, are also being implemented in our operation.

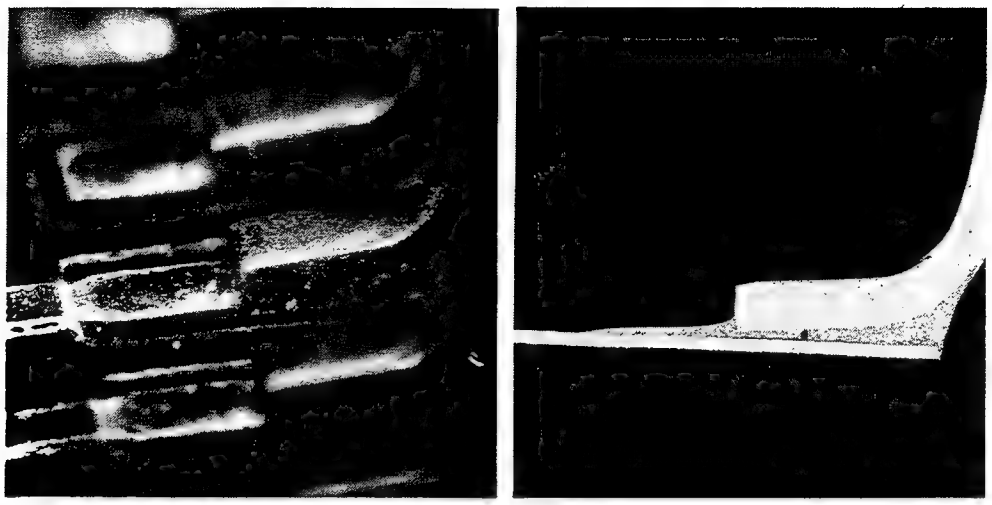


Figure 1. Typical non-tinned, probably oxidized, non-solderable gull-wing toe-end solder fillet, and cross-section of the solder joint

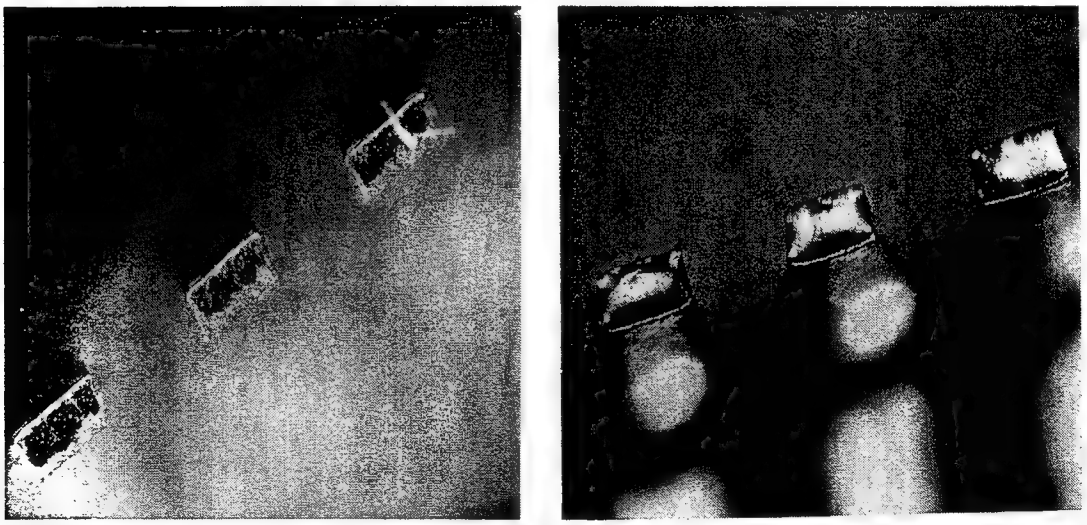


Figure 2. Two toe-end cases: typical "dip-and-look" failure, probably non-solderable at assembly; and typical "good" tinned toe-end

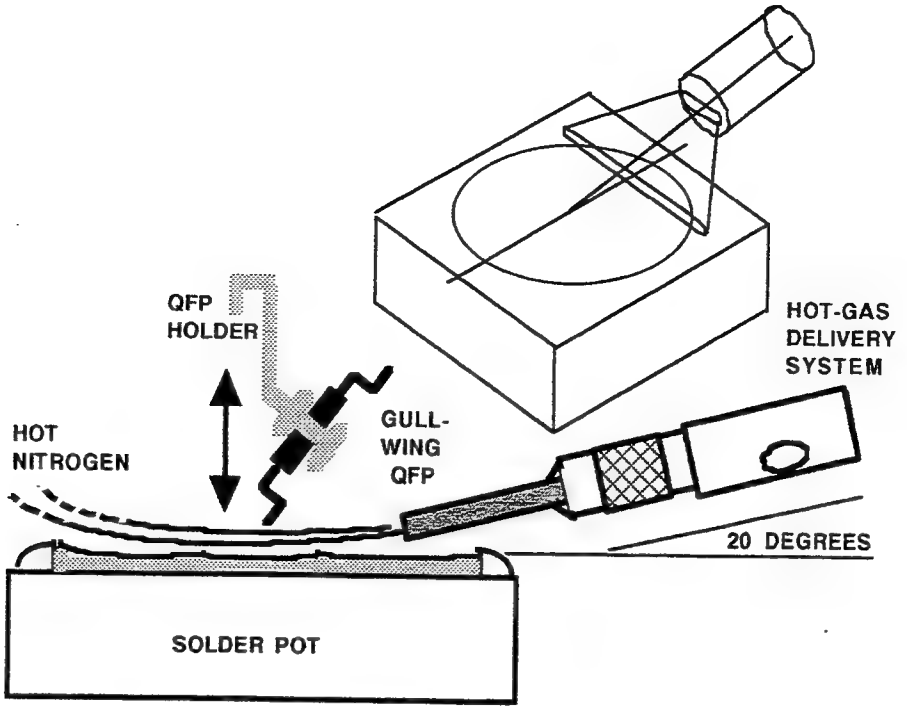


Figure 3. Sketch of the special hot nitrogen knife pre-tinning set-up

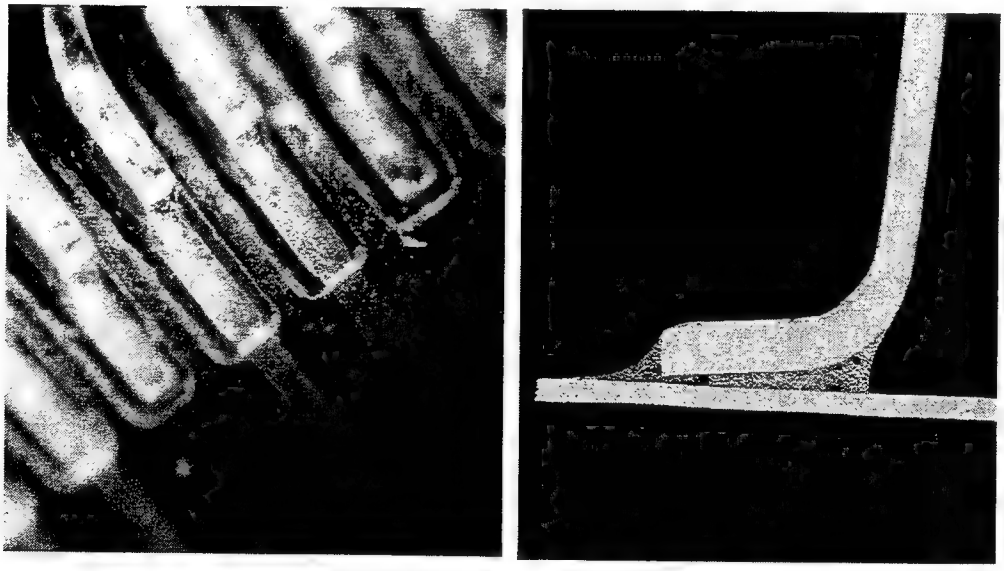


Figure 4. typical solder joint and cross section, from a successfully salvaged, pre-tinned, solderable gull-wing lead toe-end.

Tom Clifford is a Process Specialist for Lockheed Missiles and Space Company. He has 15 years' experience in plastics product and process development and 15 years' experience in electronics product development and manufacturing. He has several patents for plastics processing and a patent for a board interconnect device.

He has a bachelor of chemical science degree from Texas Tech, Lubbock, Texas.

Address: Lockheed Missiles and Space Company
1111 Lockheed Way
Sunnyvale, CA 94286

CLEANING AND CLEANLINESS TESTING OF ELECTRONIC ASSEMBLIES USING ETHANOL PRODUCED FROM CORN

BY

D. K. Pai, G. A. Maday and D. G. Loch

Computing Devices International
3101 E 80th street
Bloomington, Mn 55425
Phone (612) 853-8025

ABSTRACT

This research targets US military and commercial electronics manufacturers. They would use existing processing equipment, but with technological breakthroughs in environmentally conscious materials and processes, to produce high quality electronic modules at a reduced cost. This would be done by using ethyl alcohol, produced from renewable and recyclable U.S. agricultural products, to replace isopropyl alcohol (IPA), made from petrochemicals, to spot clean and test electronic modules for cleanliness per MIL-STD-2000(A). This paper describes the experiments conducted to evaluate the feasibility of replacing IPA with ethanol produced from corn.

SUMMARY

Computing Devices International (CDInt) has been researching techniques to develop and control environmentally safe soldering and cleaning techniques for military electronics since 1985. We have developed and patented " A Method for Cleaning Process Control" (U.S. Patent No. 4905371, D. K. Pai) and "A Method to Evaluate the Effectiveness of a Cleaning System for High Density Electronics" (U.S. Patent No. 5312536, D. K. Pai et al.), and submitted several disclosures.

During 1994, CDInt conducted research to evaluate the feasibility of replacing IPA, made from petrochemicals, with ethanol produced from corn, a renewable and recyclable U.S. resource, to clean electronic modules and test for cleanliness per MIL-STD-2000(A). The experiments were conducted using pure, drinking grade, ethanol. Based on the preliminary results of the experiments, the ethanol could provide a viable, environmentally safe alternative to IPA for cleaning and cleanliness testing of electronics. However, more research is needed to select environmentally safe denaturing additives and evaluate their impact on the long-term reliability of the electronics.

Successful commercialization of this research would have a very positive impact on the environment. The electronics industry will be a using relatively safe solvent produced from U.S. renewable and recyclable agricultural resources. This would minimize most of the problems associated with imported crude oil and petrochemicals.

BACKGROUND

Some of manufacturing processes used in the electronics industry are not environmentally conscious. The problems are primarily caused by several manufacturing processes and materials that have been developed over decades and are used almost universally in military, as well as commercial, manufacturing. One of the hazardous materials is isopropyl alcohol (IPA). The electronics industry, both military and commercial, uses several thousand barrels of IPA to clean printed wiring boards (PWB) and circuit card assemblies (CCA), and to test for cleanliness per MIL-STD-2000(A). Although most of the IPA used during cleaning is exhausted into the atmosphere, which adds volatile organic chemicals (VOC) to existing air pollution problems, a fairly large portion is mixed into the factory air and finds its way into employee respiratory systems.

Disadvantages of IPA

IPA is produced from crude oil, a non-renewable and non-recyclable resource. During 1995, the U.S. is expected to import more than 55% of its

crude oil from foreign countries. The dependence of the electronics industry on imported oil carries a heavy hidden price tag that includes military commitment to ensure a steady flow of oil, U.S. casualties in service, environmental damage caused during processing and shipping, increased health care costs due to the relative toxicity of solvents, and a $ 60 billion annual increase in our balance of payment deficit. If these factors are taken into account, the hidden price of imported oil may very well exceed $ 125 per barrel. The threshold limit value (TLV) of IPA is 400 parts per million (ppm).

Advantages of Ethanol Produced from Corn

CDInt's proposed ethanol-based processing would eliminate or greatly reduce environmentally hazardous conditions created by IPA-based processing techniques. Ethanol is produced from corn, a renewable and recyclable U.S. agricultural resource. Currently, the 39 processing plants in 20 states produce approximately 1.3 billion gallons of ethanol from corn and blend it with gasoline for automobile fuel.

The processing of one bushel of corn yields 2.5 gallons of ethanol, 15.4 lb of high protein feed stock (used by livestock and poultry farms), and 17 lb of carbon dioxide (used in carbonated beverages). These products are environmentally safe. Capacity can be increased significantly by planting more corn and producing ethanol from other farm products, such as off-grade or damaged grain, beets, potato wastes, and cellulose. The TLV of ethanol is 1000 ppm, which makes it relatively safe to use. Ethanol can be easily redistilled and recycled. Additional compelling benefits to national security are: 1) less dependence on imported oil; 2) less toxic work environment, which translates into lower health care costs; 3) expansion of the U.S. agricultural base; and 4) a great opportunity for export and positive trade balance.

The Shortfalls Associated with Competing Technologies

There are relatively few environmentally safe options for cleaning and cleanliness testing of electronic assemblies. The shortfalls are briefly described in the following paragraphs.

The use of deionized (DI) water for cleaning is the least hazardous method. However, the DI water does not remove non-ionic contamination. Water can not easily penetrate small gaps (50 microns or less) and clean contamination due to relatively high surface tension. Additional heat or hot air/nitrogen drying is required due to water's slow drying rate.

Some organic solvents (chlorinated hydrocarbons, ketones, aromatics, and esters) are very effective in cleaning non-ionic contamination. However, these solvents are toxic and will attach some of the parts and materials used in electronic assemblies.

Alcohols can clean ionic and non-ionic contamination. Methyl alcohol, made from natural gas or coal, is toxic (TLV=200 ppm) and attacks some of the organic materials used in electronic assemblies. Most other alcohols, made from petrochemicals, are relatively toxic and expensive.

EXPERIMENTS

CDInt conducted the following "limited" experiments to investigate the feasibility of replacing IPA with ethanol to test PWBs for cleanliness per MIL-STD-2000(A).

The test vehicle was SEM-E size (5.2 x 5.8 inch) FR-4 PWB, fabricated at CDInt, with an Sn63:Pb37 plated surface layer. The sample size was 20 PWBs for each experiment. Alpha Metals Ionograph 500 M was used for contamination testing. The "controlled contaminant" used in the experiments was NaCl salt solution in water.

Prior to the experiment, all PWBs were cleaned in an in-line solvent cleaning system, followed by DI water cleaning and cleanliness test per MIL-STD-2000(A). All PWBs were handled carefully by their edges, using clean gloves to minimize "uncontrolled contamination". Three drops of "controlled contaminants" were applied to the solder-plated surface of each PWB, followed by oven drying at 100°C for 1 hour.

The first set of 20 PWBs was tested, one at a time, in Ionograph per MIL-STD-2000(A) using IPA and DI water. The amount of contamination removed was recorded at the end of 2, 4, 6, 8, and 10 minutes.

The solvent (75% IPA and 25% DI water) in the Ionograph was replaced with 75% ethanol (100% pure, drinking grade, produced from corn) and 25% DI water, and the test was repeated for the next set of 20 PWBs.

CDInt repeated the above experiments with IPA and ethanol using 1 x 3 inch glass slides and a controlled amount of contaminant.

RESULTS AND CONCLUSION

The results of the above experiments using SEM-E size PWBs are shown in Figure 1. The results at the end of 10 minutes were compared using statistical "t" test at 5% alpha area. The computed value of "t = .456" is less than "t(.05) = 1.69". This means the ethanol performed as well as IPA in contamination testing per MIL-STD-2000(A). The results of the experiments using glass slides also confirmed this conclusion. Ethanol, produced from corn, provides a viable, environmentally friendly alternative to IPA, produced from petrochemicals, for cleaning and cleanliness testing of electronic modules.

The experiment were conducted using 100% (200 proof) drinking grade ethanol. Pure, drinking grade, ethanol is very difficult to control in an industrial environment. It is also expensive, mainly due to taxes. Pure ethanol must be denatured to make it unfit for human consumption and lower cost. A large number of denaturing additives are available. More research is needed to select environmentally safe denaturing additives that are compatible with electronic materials and test equipment. It is also necessary to assess the impact of these denaturing chemicals on the long-term reliability of electronics.

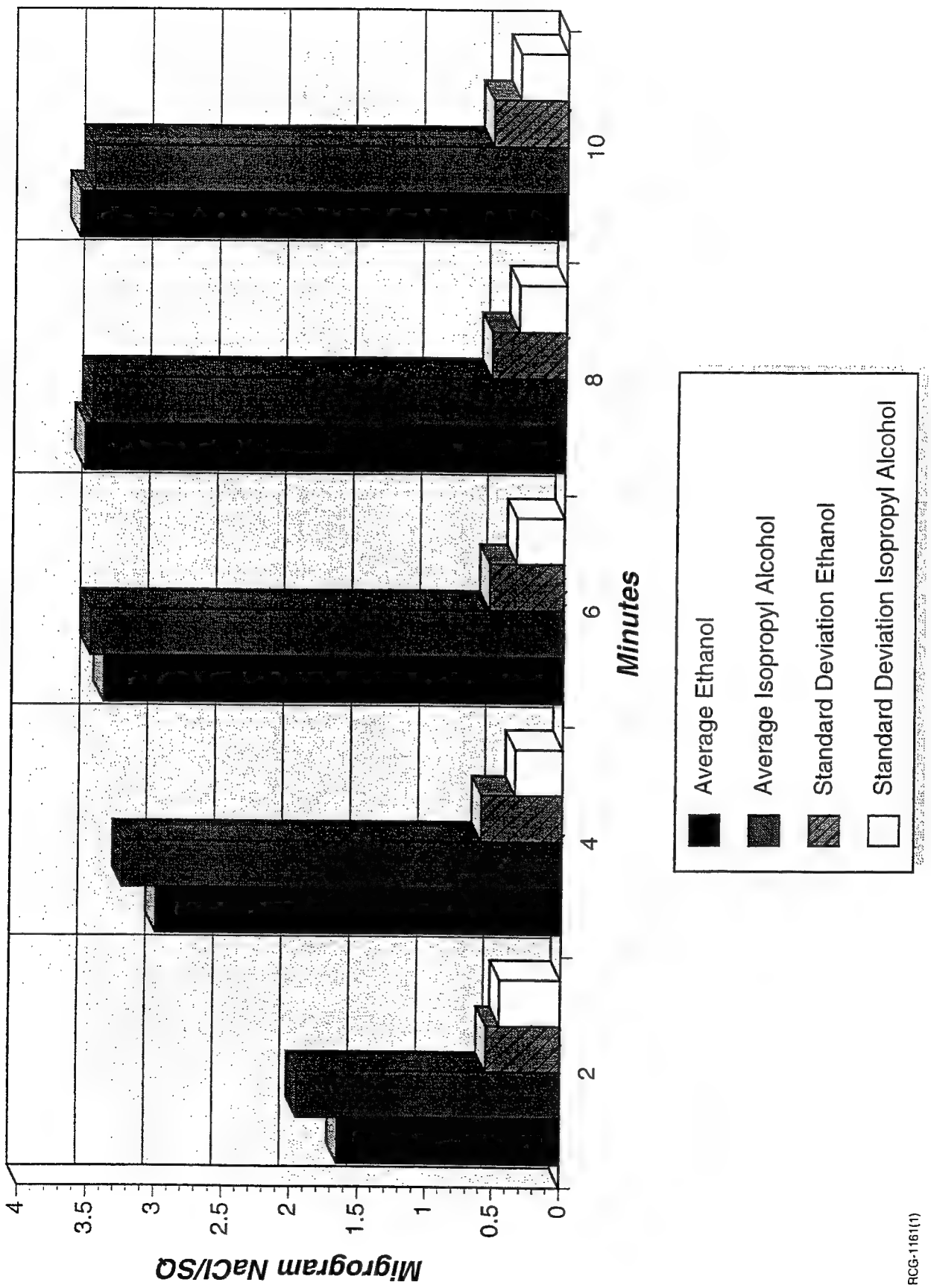


Figure 1: Ionograph Cleanliness Test Results Ethanol vs. Isopropyl Alcohol.

Deepak K. Pai is a Technical Consultant at Computing Devices International. He has 25 years' experience in military electronics and 4 years' experience in thin-film technology. He is the author of several publications on electronics technology. He holds two U.S. patents, two international patents, and has four patents pending.

He holds a bachelor of engineering degree in mechanical engineering, a master of technology degree in mechanical engineering, and a master of science degree in IE/OR.

Address: Computing Devices International
3101 E. 80th Street
Bloomington, MN 55425-1502

DETECTING AND ISOLATING MANUFACTURING DEFECTS ON BOARD MOUNTED INTEGRATED CIRCUIT DEVICES UTILIZING SIMPLE TRANSISTOR TEST TECHNIQUES

by

Jack Ferguson
General Manager
ITA Corporation
El Toro, California

ABSTRACT

The proliferation of large pin count ICs and surface mount technology have been the cause for a substantial increase in manufacturing induced defects associated with circuit board manufacturing. With the use of in-circuit functional test methods for ICs rapidly becoming ineffectual for detecting this class of faults because of IC complexity, a new patented test technique was discovered, called ChipScan, that uses a simple analog measurement technique to address this test requirement. With ChipScan, the continuity between I/O pins can be verified using a simple three pin transistor test, regardless of the contents of the IC. By scanning around the IC and using each active pin of the IC at least once in a transistor test, any I/O related defect can be detected. This article describes the ChipScan IC test technique that has been used successfully in high volume circuit board manufacturing as well as field repair environments.

CHIPSCAN IC TEST TECHNIQUE

With the growing use of surface mount technologies, continued reduction of lead spacing for mounting IC devices on circuit boards, and the increase in pin counts on packages well into the hundreds for many of today's complex ASICs, the probability for faults to exist goes up dramatically. Conversely, the ability for conventional in-circuit functional test techniques to effectively detect, let alone isolate, these faults is just as dramatically going down. This is probably the biggest problem facing test in circuit board manufacturing and field repair today. A process was discovered over two years ago, labeled ChipScan, that can detect and isolate IC faults using a simple analog measurement technique that is just as effective on simple ICs as it is on the most complex ASICs manufactured today.

CHIPSCAN OVERVIEW

The ChipScan technique makes use of the inherent bipolar transistor effects that exist between I/O pins in monolithic ICs. Test are performed without applying power to the board and without the need to backdrive ICs, as normally required for in-circuit functional test techniques. Programming effort is minimal, since it is not necessary to model the ICs or know their functionality. To test an IC, a simple three-pin transistor test is performed and then repeated around the device until all pins on the device have been subjected to at least one three-pin test. By properly biasing the pins used in each test, an active transistor current can be generated and measured, establishing continuity on all three of the pins. The only requirement to perform a ChipScan test is to have access to the net on the board that an IC pin is connected to. Consequently, conventional in-circuit bed-of-nails fixtures can be used without modification, as well as fixturless connection techniques such as flying probe systems, because only three pins at a time need be accessed to effect a test. With the use of ChipScan, a simple In-Circuit Parametric Test Technique, test coverage can be increased while simultaneously reducing the cost of test.

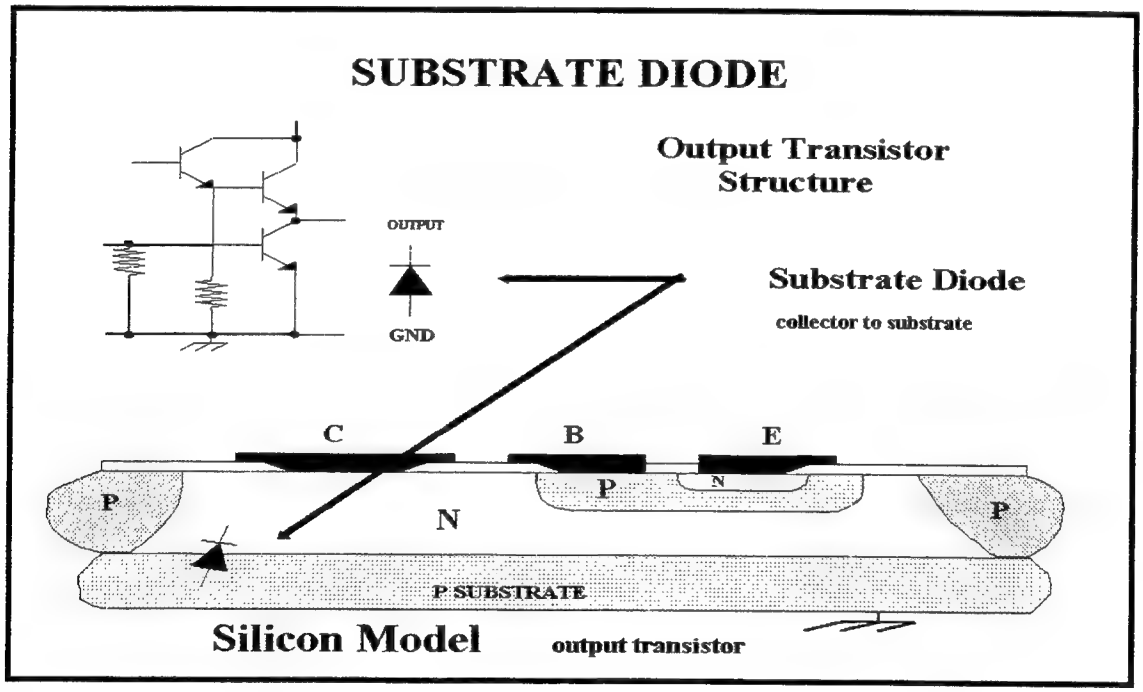


FIGURE 1. Substrate Diode at the Output Pin of a TTL Circuit Design.

PARASITIC TRANSISTOR EFFECT

The ChipScan effect works on all types of circuit technologies including TTL, CMOS, ECL, PMOS, etc. For the purposes of this discussion we will focus on TTL and CMOS

which constitute most circuit designs in production today. To form a transistor, two PN junctions are required with one of the doped regions common to both junctions, i.e. NPN or PNP. This means that a diode junction needs to exist at each I/O pin for a transistor effect to occur between those pins. The monolithic nature of the construction of ICs dictates that each transistor diffused into an IC substrate will be isolated electrically from every other transistor by a substrate diode as long as the substrate itself remains at the proper electrical potential. Figure 1 shows the general nature of a substrate diode for the output structure of a TTL circuit design. By combining an output substrate diode with the diode at the input of a TTL circuit design, as with the Inverter circuit shown in Figure 2, D1 and D2 can be combined to form a "transistor" equivalent model. In this example, the input and the output become the emitter and collector respectively of a transistor with the substrate as the base. Whether the input is called the emitter or the collector is irrelevant since a transistor effect will occur regardless of which pin is used as the emitter. Likewise, the effect can be realized between two output pins or two input pins if necessary.

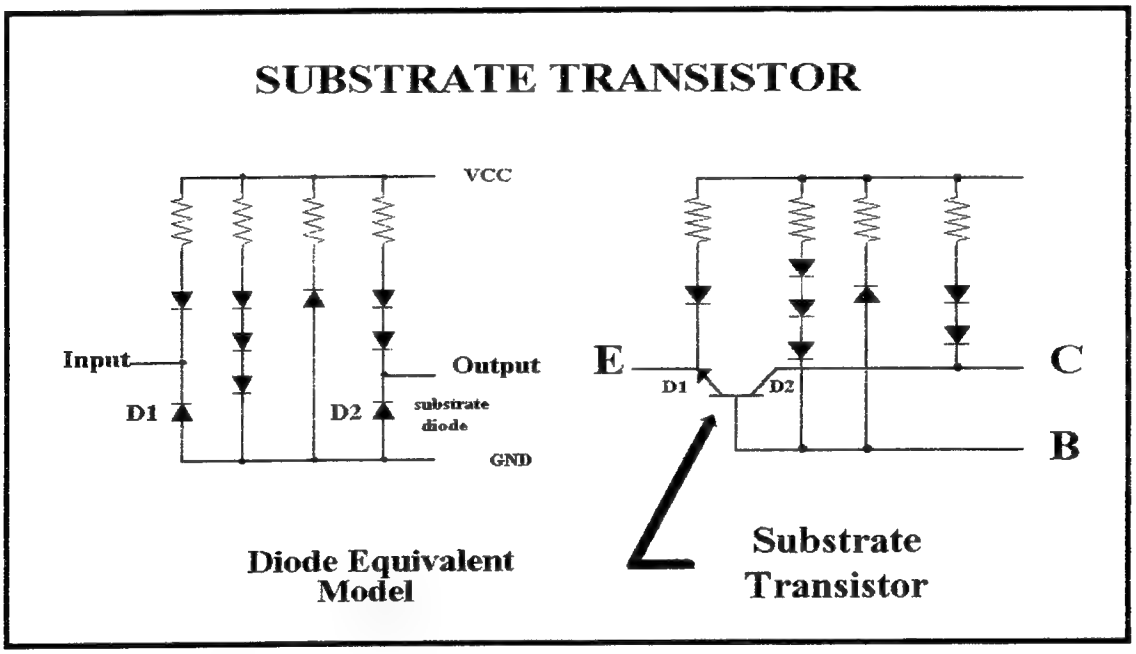


FIGURE 2. Substrate Transistor Formed Using the Input and Output Diodes of an IC and the Substrate Pin (Generally the Ground Pin).

The ChipScan transistor effect is best understood by examining the cross section of an IC. Figure 3 shows a simple example of a TTL circuit made up of two transistors and a diode. In this example, a transistor effect can be realized between the Output Transistor N doped collector region, the Substrate P doped region, and the Input Diode N doped region to form an NPN transistor. If these regions are biased as shown through the application of voltage applied via in-circuit nails making contact to the circuit board nets, then a transistor

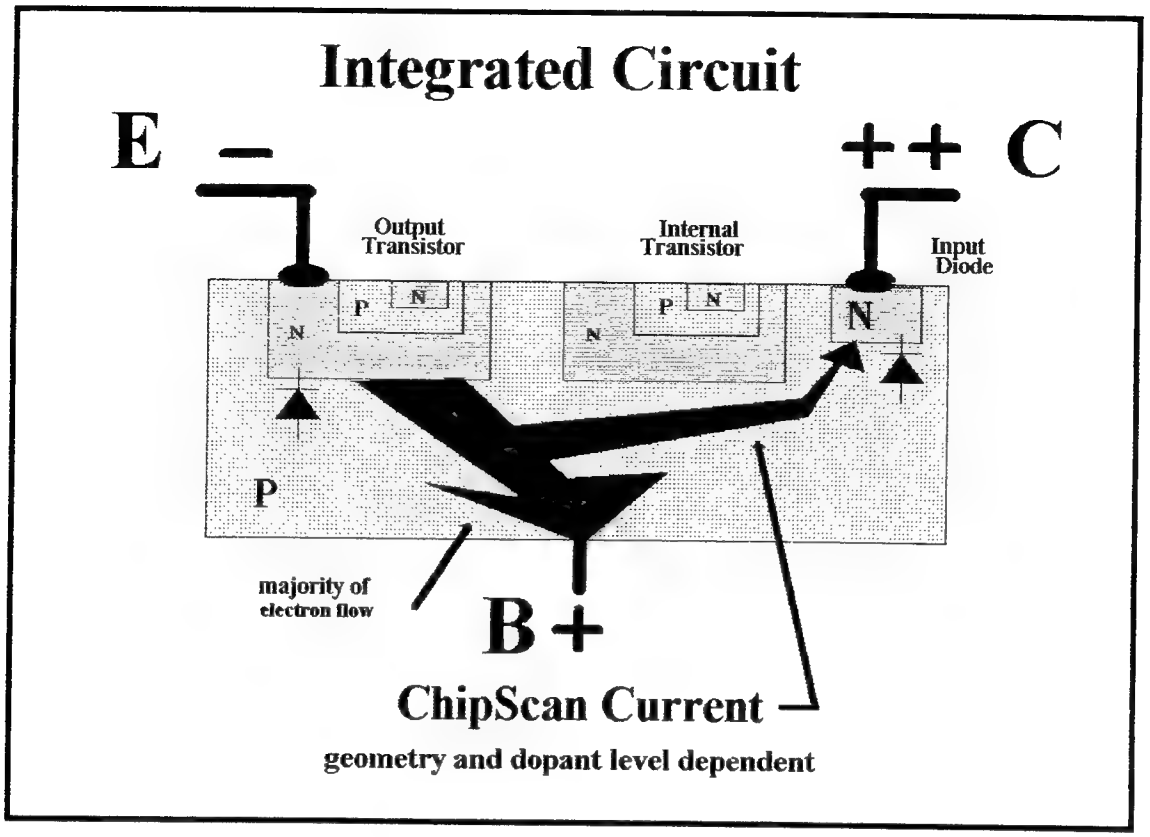


FIGURE 3. The Cross Section of an Integrated Circuit Showing the ChipScan Current as a Result of the Biasing Indicated.

current can be measured in the Collector node C, which we call ChipScan current. If any of these three pins is not making electrical connection, no current can be measured in the collector. This test then isolates an open pin down to one of three pins on the IC. By scanning around the IC using each pin at least once in a ChipScan transistor test, every pin can be checked for proper connection and deductive logic will isolate a failure to a specific pin.

The magnitude of the ChipScan current measured is dependent on the doping levels of the regions involved and the geometrys of the junctions between those regions. Figure 4 shows the collector curves for a typical TTL device using different base drives. The magnitude of the gain of a ChipScan transistor is generally much less than 1 as shown here. The magnitude is not a concern, only the presents or absents of a current. Because ChipScan currents are not a specified parameter from the IC manufacturers, they must be learned empirically from actual parts, either in-circuit or from stand alone devices. The learning process is the same for a 400 pin part as it is for a 16 pin part. Consequently, programming can be accomplished with technician level expertise regardless of the complexity of the devices involved. In numerous comparisons of the ChipScan learning

technique to other methods of board test programming, ChipScan has been shown to reduce programming time by a factor of 1/4 or more while increasing test comprehension.

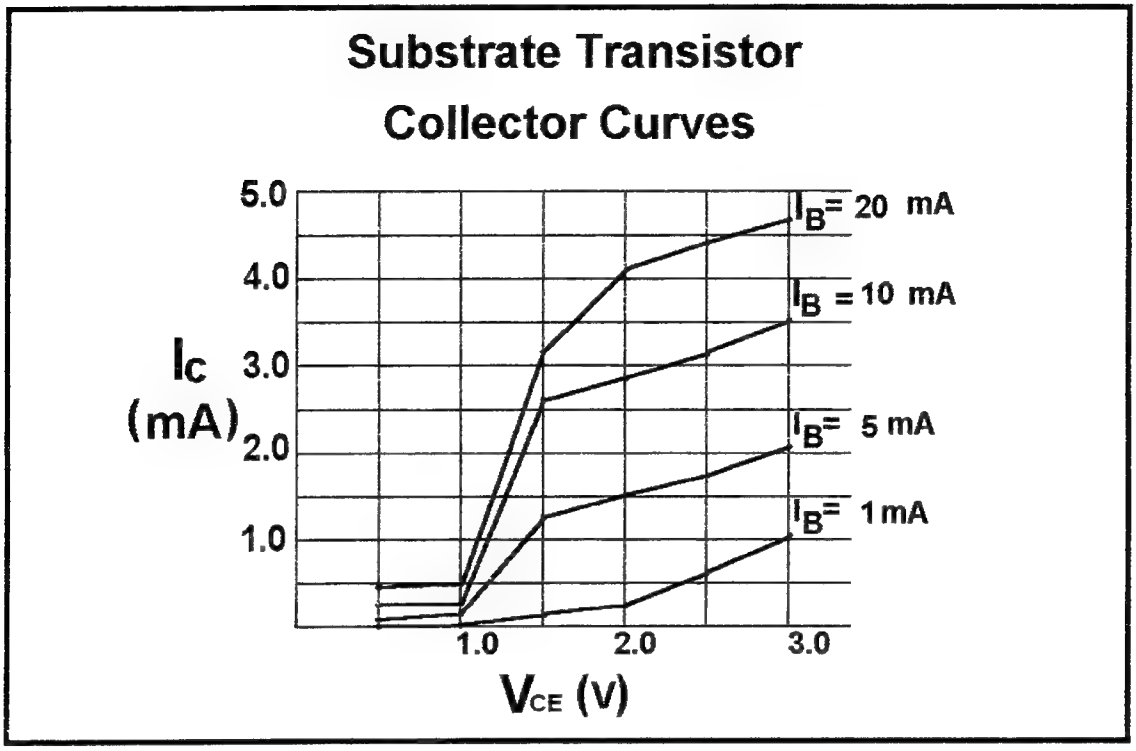


FIGURE 4. Transistor Collector Curves Between Three I/O Pins of a TTL Integrated Circuit.

IN-CIRCUIT ISOLATION

Inherent in the usage of a three pin transistor test is the ability to isolate a pin fault on an IC from the other pins on a bus. Figure 5 shows an example of three TTL devices connected on a bus. In this example, the ChipScan transistor in IC1 is being tested. No power is applied to the Vcc line, only the voltages on the pins as shown. In order to turn on the substrate transistor in IC1, the bus is placed at a higher potential than the ground lead. Consequently, the substrate transistors in IC2 and IC3 are back biased so that no current can flow into those leads. Whether there are two ICs in the fan out or two hundred, the only place current can flow is in the substrate transistor of IC1. Therefore, if no current is detected in the collector lead, than one of the three pins on IC1 is faulty. For TTL designs, this process is simple and pure because of the diode isolation from the I/O pins to the Vcc line. For CMOS devices, the process gets a little more complicated.

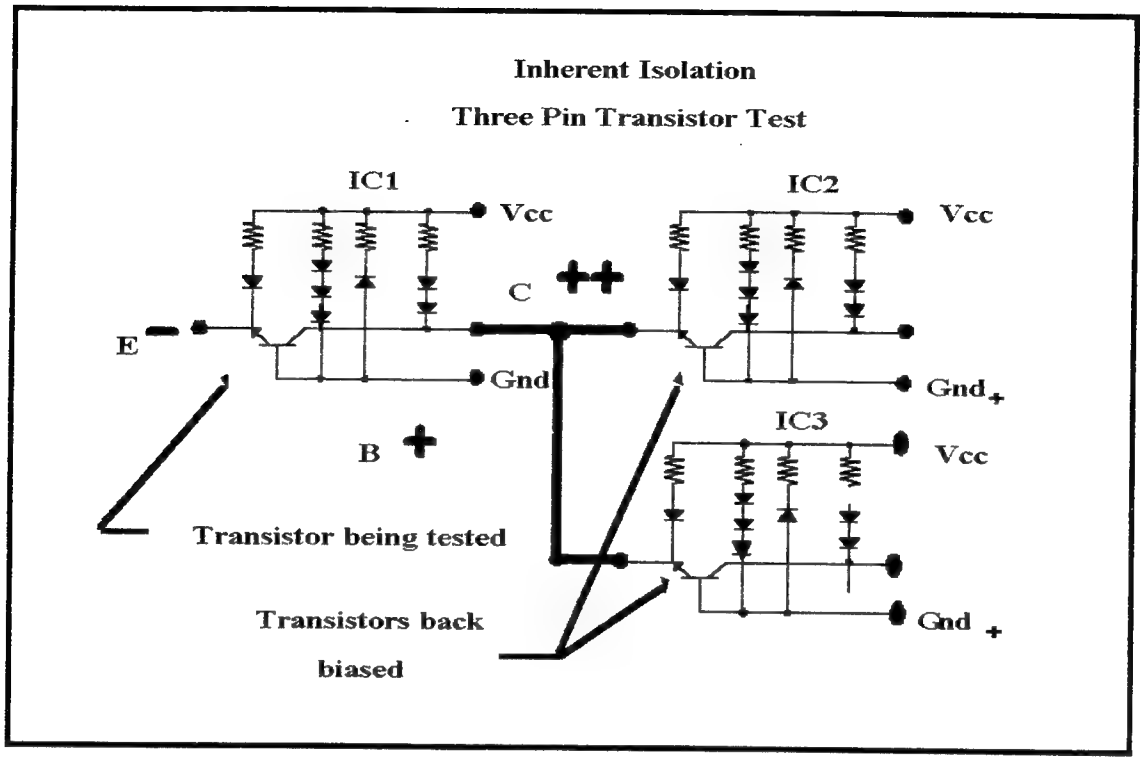


FIGURE 5. Inherent Isolation Using a Three Pin Test for Bus Structured Circuits

CHIPSCAN AND CMOS

For CMOS designs, diodes at the I/O used for static discharge suppression as well as to inhibit latch-up provide a means for implementing a ChipScan effect. Figure 6 shows the I/O model for a simple CMOS Inverter circuit. The unique feature of CMOS with respect to ChipScan is that the suppression diodes provide a forward bias to the Vdd terminal that is not present for TTL devices. Consequently, if the circuit in Figure 5 is replaced with CMOS devices instead of TTL devices, another path besides the ChipScan transistor path becomes available for current to flow from the collector lead, that being through the Vdd terminal. This Vdd current is referred to as background current and must be accounted for in order to measure the presents or absents of ChipScan current.

Several techniques have been devised to eliminate this background current (patents pending). With these current compensation methods, CMOS devices can be tested using ChipScan with the same effectiveness and reliability as with TTL devices. This

background current problem was most prevalent when trying to test circuits where a variety of vendor devices were used in the same location on a circuit board. As might be

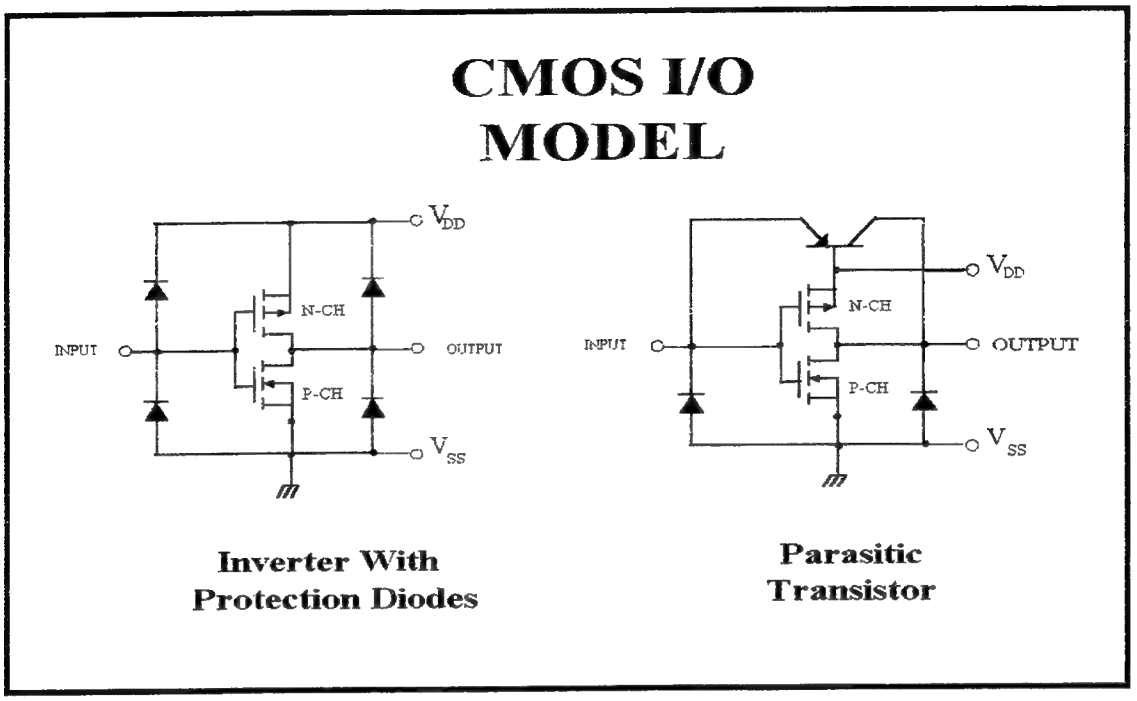


FIGURE 6. CMOS I/O Model With Protection Diodes That Are Used to Establish ChipScan Transistors.

expected, the absolute value of the currents measured on the same pin in a specific device in a given circuit between different vendors can vary quite dramatically. Figure 7 shows just how dramatic this variation can be. The white bars show the amount of ChipScan current measured on the same pin across different vendor parts in the same circuit. The black bars at the bottom of each white region show the current measured utilizing background current compensation if the pins are not making electrical connection. Effectively, no current flows if a pin is open, no matter which vendor part is inserted in the circuit. Consequently, ChipScan is immune to vendor or lot-to-lot variations in the absolute value of the current measured.

COLD SOLDER JOINTS, STATIC DISCHARGE, WRONG FAMILY PARTS

One of the compensation techniques for eliminating background currents involves comparing the current values of like function pins on an IC. This technique, called Grouping, provides the added benefit of being able to detect the presents of a cold solder joint as well as open pins. A cold solder joint causes the current to be attenuated with respect to like pins on the IC, thus creating a failure. The grouping technique is based upon the fact that, although the absolute magnitude of the currents measured from vendor

to vendor may vary by an order of magnitude or more, the relative relationship between like function pins on an IC remains constant, regardless of the vendor. Consequently, this relationship can be learned on any of the vendor parts and the test will automatically

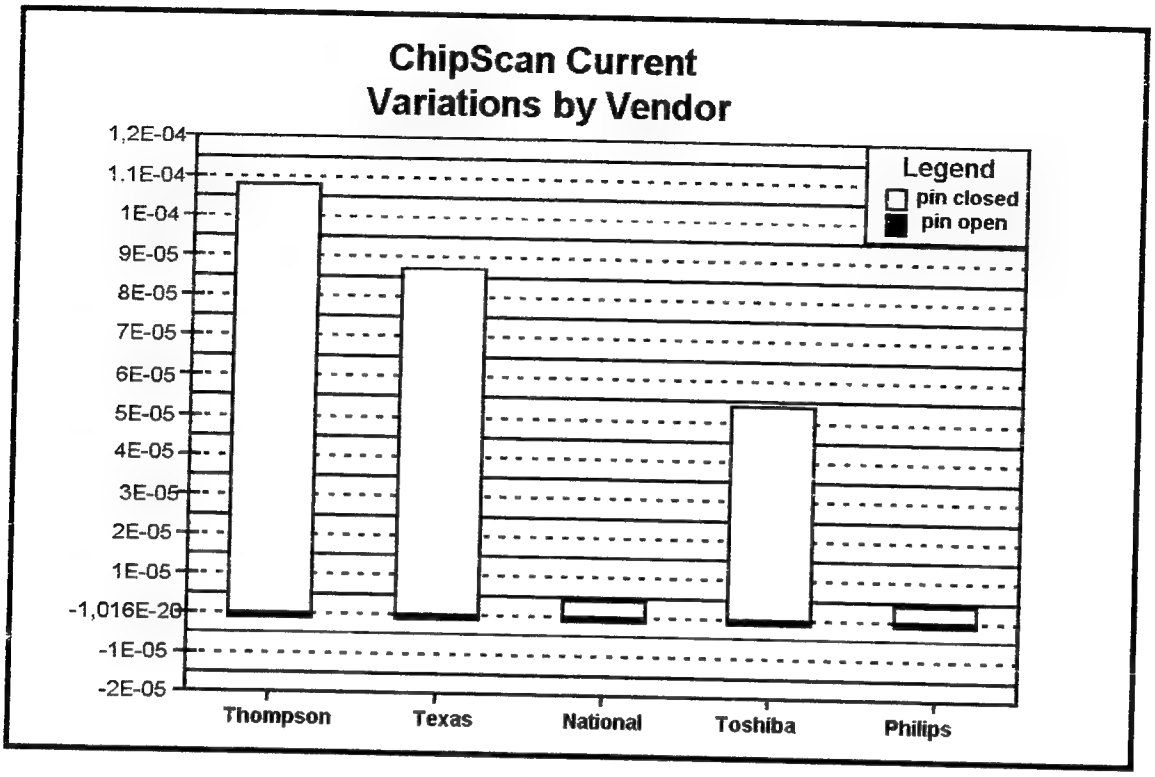


FIGURE 7. Vendor Variations in the Absolute Value of ChipScan Currents For Pin-for-Pin Replaceable Devices as Measured In-circuit. The Black Bars at the Bottom of Each White Bar Shows That Zero Currents Are Measured for Open Pins for All Vendors Parts Regardless of the Good Connection Current Magnitude.

adjust for a different vendor part being tested. Static discharge failures can also be detected because they short the base to emitter or base to collector junction as a result of a "punch through" in the gate oxide region radically altering the expected value. The ChipScan technique has also been very effective in detecting the presents of the wrong family of a device with the same function, i.e. 74LSXXX versus a 74SXXX.

CONCLUSION

ChipScan was the first Parametric In-Circuit Test Technique to be used to test for open pins on IC devices where in-circuit functional test techniques were no longer viable or economically effective. It is a simple technique that can be programmed by technician level personnel and without special fixturing considerations or knowledge of the function of the IC. It works on all types of circuits, including CMOS, and it has the added benefit of being able to detect not only open pins but cold solder joints and wrong family devices. Because it requires a maximum of 4 pins at time utilizing a scan technique to test any size IC, ChipScan can be implemented with a Flying Probe interface system to further reduce costs or to provide testing of boards where access is too limited for a conventional bed-of-nails interface due to circuit densities.

ChipScan is the application of basic physics, taking advantage of the monolithic structure of today's most complicated Integrated Circuit designs. When ChipScan is used in conjunction with a high performance Parametric In-circuit Test System, all types of manufacturing induced defects or field return defects associated with I/O failures of devices can be detected at a significantly reduced cost without sacrificing test coverage, and in many cases can increase test coverage.

Jack Ferguson is General Manager of ITA Corporation. He has been involved in IC failure analysis and circuit testing for the past 25 years.

He has a bachelor of science degree in physics from San Diego State University.

Address: ITA Corporation
24582 Via Del Rio
El Toro, CA 92630

THE PROBLEMS ASSOCIATED WITH ADHESIVE BONDING OF COMPONENTS ON SURFACE MOUNT ASSEMBLIES

by

George S. F. Orsten, Senior Staff Scientist, RDD;
Lockheed Missiles and Space Company
Sunnyvale, CA.

ABSTRACT

The bonding of any component onto an SMT assembly is usually undesirable from the standpoint of the manufacturing organization. It is often necessary however, either because a thermal path is required from the integrated circuit or hybrid part down to the substrate, where a voltage plane can be put to dual use by making it serve as a low resistance thermal path off the board as well, or because the vibration environment is such that a gullwing type chip will probably flex enough to cause crack failures of the leads.

The choice of thermal and/or mechanical properties has to be considered, but this is far from the only considerations of the adhesive used. Cure schedules are important, and the question of necessary pre-cure arises, since the process of bonding intrudes into the normal SMT schedule of building. The possibilities of expansion during cure must be considered, which would tend to raise the leads out of the solderpaste on the lands.

This paper describes much test work, and many problems that were overcome, as well as showing the strength of normal solder joints found in chip applications, and their relevance to survival in various G level environments during testing and use.

INTRODUCTION

It is often necessary to place adhesives under larger integrated circuit packages for reasons of vibration survival or providing a thermal path to the board which may have a fairly thick (2 oz) copper plane layer on top to carry heat to the edges of the assembly. The use of such an adhesive can lead to many complications, and the choice of materials, methods, and layout patterns for the lands all must be considered.

It is instructive to remember exactly what happens in an SMT assembly as the solder joint is formed. A layer of solder paste is applied to the land surface, perhaps 5 mils thick.

The part is placed, hopefully accurately on the lands, but actually semifloating on the solder paste. The assembly is heated to reflow temperature, at which point the solder loses a part of its volume, because of flux volume loss and solder ball amalgamation as it melts. The part follows the solder down, and ends up much lower than the initial 5 mils. In the process, the solder joint geometry is determined, particularly with respect to heel and toe fillets. The steps in this process are shown graphically in Figure 1. If anything is done to disturb this "naturally occurring" process, the results will not be the same, and may not be at all to the liking of the engineer responsible!

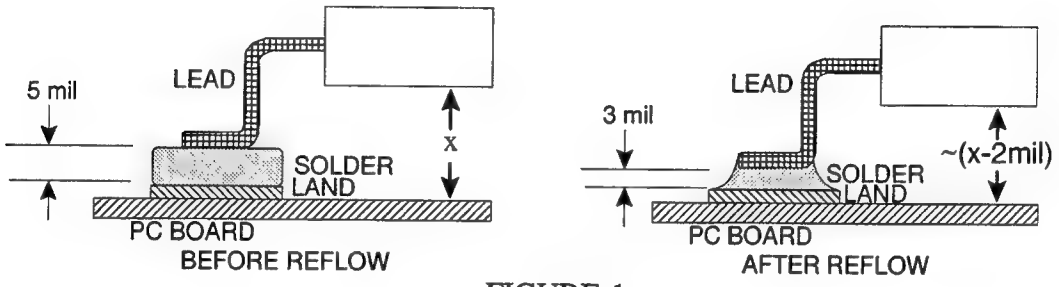


FIGURE-1

The possibility of having to remove this part at a later time without destroying the board or the surrounding components also raises questions. Some adhesives are next to impossible to remove without applying so much force that everything else is at risk. The fact that the solder joints have to be undone either first, (and without the possibility of moving the part), or at the same time as the breaking of the bond does not endear this whole process to the industry. Undoing a solder joint without moving the part implies totally removing all solder; an obvious impossibility. Unsoldering the joint at the same time as breaking the bond requires a rework machine that to the best of my knowledge, simply does not exist. Even the most sophisticated equipment such as the SRT machine that costs about $120K with all the accessories and options, can still only put a few grams of force on the body of the part, using a tiny nozzle and a vacuum system. We must also try to satisfy the occasional ultra-optimist who thinks he can save the removed part and reuse it, even when it is a fine pitch 20 mil part that has a few hundred leads!

DISCUSSION

It goes without saying that the adhesive chosen must have a high thermal conductivity. Assuming a chip that is about 3.3 cm on a side, and leads formed to have a standoff height of 3 mm, you have an area of 10^{-3} m^2, and a adhesive thickness of 3 x 10^{-3}. With an adhesive that has a conductivity of 3.6 w/m-°C, the heat transport is excellent, you have:

$$\frac{3.6 \times 10^{-3}}{3 \times 10^{-3}} = 1.3 \text{ W/°C}$$

Recognize however, that this would be an excellent adhesive, in fact one of the best, and this assumes 100% coverage of the adhesive over the area of the chip. That area coverage is very hard to achieve. Place enough adhesive under the chip for total coverage, and it may squeeze out onto the land and solder area. A coverage of 50% is much more realistic. Also, many adhesives have a conductivity value of 1/6 of that in the example, and are still considered good thermal bonding materials. Fillers used to achieve these kind of numbers are aluminum nitride or even diamonds. All are abrasive, and result in a great deal of wear to the positive displacement pumps that are needed for accuracy in placing the right amount of material on the board. Many of these pumps, on the best of units, operate by means of an Archimedes screw driving the material, just like a meat grinder. What is needed is a cross-breed between this and the simple time-pressure pumps you find. A fine lead-screw driven by a stepper motor, which then puts pressure directly on the piston of a simple syringe barrel would give the accuracy of positive displacement, and almost total lack of wear, as the cylinder and piston are discarded when empty. No one, to our knowledge, makes such a device, even though it seems intuitively obvious.

The adhesive must not lift the component off the board by any significant amount, either at the time of cure if the material is to be cured just before reflow, or during reflow, cured or uncured! In reality, almost any epoxy will cure at least partially just in the heating it gets from the reflow process temperatures. Lift comes from entrapped air, outgassing solvents, and from the C_{te} of the material itself. Entrapped air comes either from bad patterning on the board or poorly mixed two component material that has not been degassed after mixing. It may exist even with single component materials direct from the manufacturer, if they are not properly degassed at the factory, a process that is not inexpensive on an assembly line, and one that you should expect to pay for. C_{te} is a characteristic of the material, and needs to be measured. Don't trust the vendor on this specification. Outgassing from volatile components of the adhesive mixture are also characteristics you will need to check for yourself, the vendor won't know, or won't tell you. Also recognize that the C_{te} of fully cured material may be quite different than that during the cure, or after a partial cure. A small amount of lift is actually desirable, since at reflow temperature it lifts the component up, the solder then solidifies just below 183°C, and now the adhesive contracts as the assembly cools. This leaves a net compressive force on the solder joint, something highly desirable for long cyclic life. But the amount of lift cannot be so much that there is inadequate solder volume when the joint is formed.

The actual lift we have seen varies greatly with the adhesive chosen. With the cure schedule recommended by the vendor, we have seen values ranging from 1-2 mils, up to 7-8 mils. The latter values are clearly unsuitable, as it is impossible to get enough solder in there to fill the space properly. The following chart shows a representative group of adhesives, tested by having a formed 16 pin flatpack placed on a bare substrate with

adhesive at the center, but without lands or solder, and then going through the normal cure. The lift is given as two numbers, taken at 2 corners. One is the highest, the other the lowest lift for that chip.

ADHESIVE TYPE	SAMPLE-1 LIFT	SAMPLE-2 LIFT	SAMPLE-3 LIFT	SAMPLE-4 LIFT
A	3,8	2,9	3,11	
B	2,6	1,1	1,1	
C	0,5	2,8	1,6	
D	0,1	0,1	2,2	1,1
E-pattern-1*	4,6	3,8		
E-pattern-2*	1,1	0,2		
	*Pattern-1; Lines		Pattern-2; Matrix of dots.	

The parts, as can be seen from the table, are usually no longer parallel to the plane of the board. The cure schedule will make a difference, as will pre-curing before the reflow cycle versus just setting the whole assembly uncured on the track, and letting the reflow system do what it will. The pattern can be crucial, as seen in the 2 cases for type "E" material. The wrong pattern will give both air entrapment, as well as minimizing the adhesive area exposed to the outside from which volatiles can escape. An inappropriate pattern can give rise to air entrapment and will give a sequence of events as shown in Figure 2, resulting in both a tilted and raised part. This is probably what happened to pattern-1 for material "E".

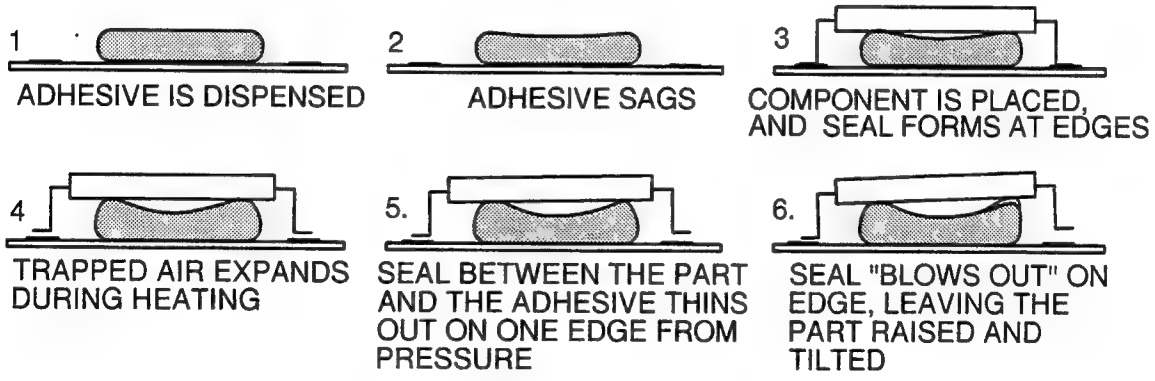


FIGURE-2

The solder joints that result from this lifting are shown in Figure-3. On the left, "A" is what you are striving for. Most of the time, you will get "B", which will be rejected under most specifications by your inspector for insufficient solder. Often, you will get "C", where the gap was too great for the solder to hold together, or the lead never touched the solder paste during reflow at all.

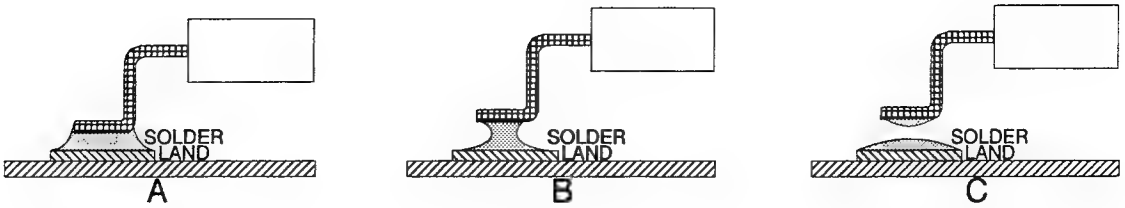


Figure-3

The material must be reworkable. Usually this is enhanced by having the assembly on a hot plate, and heating it up to somewhere near 100°C. At this point, the component can be torqued off without damage to the substrate. Most epoxies will have shear strengths of at least 1000 lb/in^2 at the temperatures that the assembly will operate. This is more than enough to protect the component from vibration and acceleration. A 1.3 in long component has an area of 1.69 in^2, and if you have 50% adhesive coverage, the shear strength will be 1.69 x 0.5 x 1000 = 845 lb. Assuming that this part has a mass of 2 oz, the part is protected up to 845 x 16/2 ~ 6800 g acceleration. At 100° - 125°C, the shear strength of the adhesive should be considerably less to allow removal. High temperature epoxies are not what you want to use here. You will need to build a machine, similar to the one shown in Figure-3 for torquing off the parts. This one, built from cannibalized parts, uses a worm drive so that a lot of torque can be exerted, but the chuck holding the chip will not over-spin at the moment the adhesive lets go. If it did, and you had a matrix arrangement of chips, you probably would damage all four parts on the sides of the part you are removing.

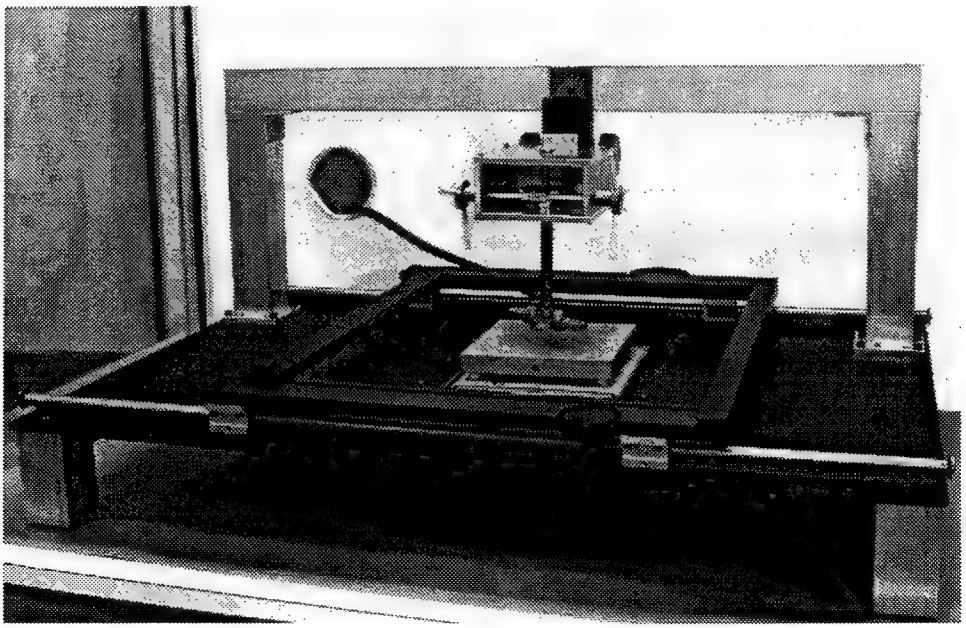


Figure-4

A closeup shows a better detail of the actual head, in Figure 4 below. The adjustable jaws which grip two opposite corners of the chip to be removed can be seen. Note the worm drive, and the relatively long triple handles on the two sides of the shaft for the worm, to allow easy application of a considerable force, sometimes necessary to remove large parts. The hotplate can be seen below, with the removal mechanism on a cannibalized microscope vertical rack and pinion system, always centered with respect to the hotplate. The P.C. board is shifted to bring the part into alignment, and the removal mechanism is lowered onto the part. With an almost pure torque applied, the center of the adhesive will fail in the classical 45° pattern, and the outer sections in straight shear. A material needs to be selected so that the residue can be cleaned off the board with relative ease.

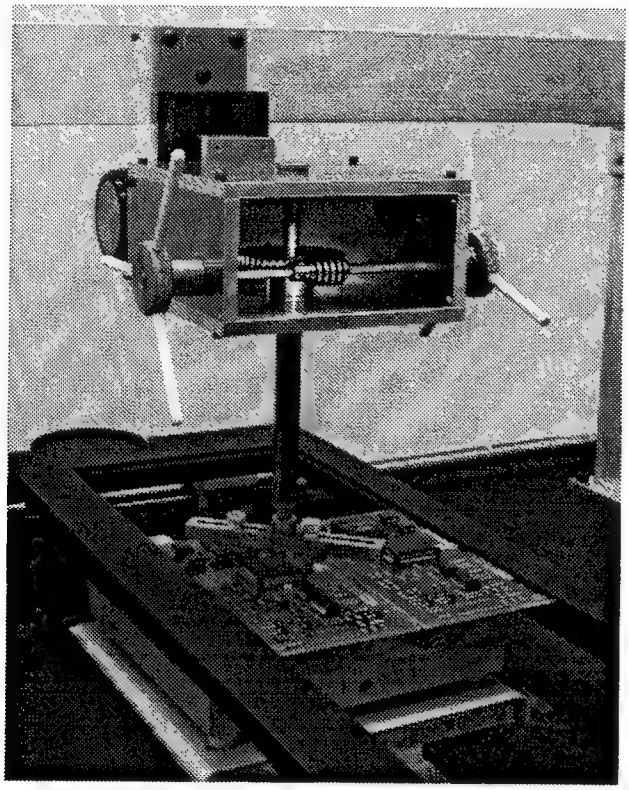


Figure-5

Finally, the pot life is important from an operational viewpoint. A one hour potlife would be a real nuisance, and if this were a two component system that needed mixing and degassing in a bell jar, you would almost have one man on the line doing nothing but mixing, discarding, degassing, and reloading adhesive! A one component system is certainly easier for the line engineer to work with, but these require cold storage, and once heated up, as they must be to get the viscosity to where you can dispense them, pot life can be quite short.

Lastly, the adhesive must withstand attack from your cleaning system, and must not outgas if you are going into space. The latter requirement will eliminate a lot of otherwise good choices.

Assuming that the right adhesive was chosen, and the right process developed around both it and the equipment used on the line, the question comes up as to the effect of the adhesive on joint life. The answer to this is that it will depend on how the assembly was made. Some people have given up on trying to get this process under control, and have left holes under the parts, in order to pump adhesive in under the part, after the whole normal SMT assembly process is done. This can lead to a large problem in temperature cycling life. The usual strain on a joint is:

$$L_D \, \Delta C_{TE\text{-}1} \Delta T$$

where:

L_D = diagonal length across the feet of the part
$\Delta C_{TE\text{-}1}$ = difference in coefficient of thermal expansion between the chip and the board
ΔT = temperature cycling that the assembly sees

But when an adhesive is pumped under the part, and then cured near ambient, it will expand when heated later on in the mission environment of the assembly, and a second ΔC_{TE} enters the strain equation. We now have a lead, possibly Kovar at a value of ~6ppm/°C, or copper at about ~19ppm/°C, and an adhesive that can be as high as 250ppm/°C, and is seldom as low as 125ppm/°C. There is a standoff height between the bottom of the component and the board, which can be anywhere from 4 to 20 mils high. So there is another strain factor,

$$\{(d \times C_{TEA}) - (\ell \times C_{TEl})\} \Delta T \times E$$

where:

d = thickness of the adhesive
ΔC_{TEA} = coefficient of thermal expansion of the adhesive
ℓ = vertical length of the lead
ΔC_{TEl} = coefficient of thermal expansion of the lead
ΔT = temperature cycling that the assembly sees
E = Young's modulus for the adhesive

which is normal to the plane of the usual stress. This strain is tending to lift the part off the board and therefore puts the solder under tension, which is not the strongpoint for solder joints! Adhesives pumped in after the fact must therefore be cured stress free at a temperature higher than any operating temperature so that the net force left over is compressive. Just as the vertical portion of the lead gives some compliance as a relief from $\Delta C_{TE\text{-}1}$ in the top equation, the horizontal lead projection out of the case gives some compliancy for the vertical C_{TE} problem. Unfortunately, we generally have no more than 0.030" before the top bend starts. A larger value would be useful for parts mounted with adhesive.

For adhesive that is applied immediately after the solder paste, usually with some sort of displacement pump device on a programmable X-Y table, the question depends on when the material is cured. If it is completely cured and stable before reflow, then the adhesive expands during reflow, the solder joint is formed, and then as the assembly cools, the joint goes into compression. The problem can be with the definition of "cured". Some very unpredictable things can happen insofar as permanent or temporary lift of a part with respect to temperature are concerned, when the material is not totally cured. Total cure, on the other hand, can be impractical if either time or temperature would impact the solder paste. It is worthwhile to undergo any cure necessary in a nitrogen environment to avoid oxidation of the solder paste.

Finally, the desirability of using adhesives under small chip components must be commented on. Aside of the almost impossible task of reworking such a component, the question of need should be answered.

We had an interesting opportunity to do a test in January of 1991. While setting up our SMT facility at the Palo Alto Research labs in 1989, we were hit by the Loma Prieta earthquake. The damage to our building was severe enough, that it was 13 months before we could get back into the building. The day of the earthquake, we were preparing to test out our equipment. We had etched a board, bare copper, no plating as yet, that would take a handful of 1206 components. We had solder paste in the refrigerator, and a box of 6 year old 1206 resistor and capacitor components, left over from another job. The board and parts were in the facility, under a laminar flow bench, ready for the test, with the stencil already mounted on the printer. Everything was there, 13 months later, when we got back in. In the meantime, there had been no HVAC system and no power for the refrigerator. The boards were greenish-black from oxidizing and sulfiding of the bare copper, the parts were already very old, and the solder paste was out of date, and had gone through one California summer without refrigeration. It was black and nasty looking. As a joke, we decided to run the test, as if nothing had happened. The solder joints will go down in history as the worst joints ever made anywhere. We then sent the boards down to the mechanical test facility, and had all the components pulled off sideways, meanwhile plotting the normal stress-strain relationship. The **lowest** value for failure from any 1206 component was 5.6 Kgm! Since this component weighs about 50 mgm, it is safe up to 5600 x 20 = 112000 g. It does not need an adhesive to hold it down!

The test was repeated about 1 year later with a flight quality P.C. board, good solder paste, and new capacitors slightly larger than 1206 size. This came about when NASA got suspicious about the quality of the terminations of some capacitors we had used, and asked us to make a spare high voltage board with 24 capacitors only, and then test them. With flight quality on everything, the lowest failure point on this same test was 15.6 Kgm. In fact, none of the solder joints themselves ever let go. In every case, the

capacitor itself was ruptured, in some cases at the end seal, and in some cases right at the center of the body, where the test hook pulled hard enough that a portion of the body came away, with two shear planes failing, one on either side of the hook, but neither at the termination. The 15.6 Kgm value came from a termination failure, where the ceramic body separated from the metal termination which remained in the solder, and on the land. The units that failed with a double shear failure averaged about 42 Kgm.

CONCLUSIONS

A few conclusions can be made from the data presented. First of all, any time that any adhesive is used before reflow, the solder joints will not be "normal", in the sense that they will be different in geometry from what was expected. In almost all cases, there will be a diagnoses of "insufficient solder". We have overcome this in three ways.

1. Make the lands longer on each end, and the solder that is deposited there in the stenciling operation will flow up into the joint because of cohesion and capillary action. About .040" to .050" should do it.

2. Parts that are pressed down into the solder paste still can not get any lower than the size of the largest solder sphere. Therefore, use finer powder solder paste.

3. Apply pressure for some time in your pick and place machine, to get rid of the bounce-back that you may have from the adhesive. The time will vary with the size of the part, for something that is perhaps 1 1/2" on a side, try 30 seconds. The force should be between 250 and 400 gms.

4. Make your stencil with a double window, so that you apply no paste under the foot, but only on the extra section of the land on each side. The small amount of bounceback will insure that you do not actually get down flush on the board with your parts, and the solder will come in from both ends during reflow.

You must know all the characteristics of the adhesive you want to use. Be prepared to make many of the measurements yourself. In particular, Young's modulus for the fully cured material is important, the shear strength is important, and the shear strength at elevated temperatures is important. We had one excellent choice for material; unfortunately, no one ever figured out how to get a part back off the board!

You will need some sort of device that can exert a controllable torque for removal of parts. Most of all, the device must not "overspin" at the moment the adhesive lets go.
Do not assume that you can get much more than 50% coverage. Greater coverage attempts result in adhesive squeeze-out onto lands, or air and possibly volatiles entrapment in the center that give very large lifting.

Be prepared that when you have found the material of your choice, there may have to be a pre-cure. If that is so, then you need an oven that has the right characteristics, and if the cure is very long or at temperatures of 100°C or higher, the parts will have to be in a N_2 atmosphere or you destroy the properties of the solder paste.

Adhesive is not needed under chip components, and can only end up with trouble by not allowing the joint to form in a normal manner including auto-alignment. In the worst case scenario with small parts such as 0506 or smaller, the adhesive could get into the solderpaste.

ACKNOWLEDGEMENTS

The contributions of several colleagues must be acknowledged. They had a major part in this work, both in having many of the basic ideas which helped us get the eventual solutions, and actually performing much of the experimentation which took place. In alphabetical order, they are Thom Clifford, Jari Drlik, William New Sr, Marc Peloquin, and Yun Wang, all of Lockheed. Mr. Clifford and Mr. Peloquin are presenting a paper of their own, on another subject, at this meeting.

George S. F. Ornsten is a Senior Staff Scientist at Lockheed Missiles and Space Company. He has over 40 years' experience in the design and building of electronic systems and devices. He has been in the space business since 1958 and has served as a member of the Physics and Astronomy Department of the University of Massachusetts for 18 years, doing research and teaching. He has produced many journal articles over the years in the *Review of Scientific Instruments*, and has given papers at SMI-92, the 18th Annual Electronics Manufacturing Seminar Proceedings in 1994, and the International Congress on High-Speed Photography 1960.

Address: Lockheed Missiles and Space Company
3251 Hanover Street, B0251, Dept 97-80
Palo Alto, CA 94304